Journal of Ceramic Processing Research. Vol. 12, No. 1, pp. 57~61 (2011)

J O U R N A L O F
Ceramic Processing Research

A study of the memory characteristics of multilayer structures with varying compositions of the La_xAl_yO charge trap

Seung-Yong Cha, Hyo-June Kim and Doo-Jin Choi*

Department of Advanced Materials Science and Engineering, Yonsei University, 262 Seongsan-no, Seodaemun-gu, Seoul 120-749, Republic of Korea

Charge trap flash (CTF) memory devices are candidates to replace NAND flash devices. In this study, $Pt/Al_2O_3/La_xAl_yO/SiO_2/Si$ multilayer structures with lanthanum aluminum oxide charge traps were fabricated for nonvolatile memory device applications. An aluminum oxide film was used as a blocking oxide for low power consumption in the program/erase operations and to minimize charge transport through the blocking oxide layer. The thickness of SiO_2 as a tunnel oxide layer was 40 Å. The thicknesses of the oxide layers were determined by high resolution transmission electron microscopy (HRTEM) and all samples showed amorphous structures. The composition of the charge trapping lanthanum aluminum oxide were analyzed using X-ray photoelectron spectroscopy (XPS). From C-V measurements, a maximum memory window of 3.48 V was observed when the flow rate ratio was La : Al = 3 : 3. The memory properties were affected by the band structure, trap energy level/density, and dielectric constant of the charge trap layer. In the reliability cycling tests, all samples maintained their initial memory window over 10^4 cycles.

Key words: Charge trap flash, $LaAlO_3$, tunnel oxide, MOCVD, SONOS

Introduction

Silicon-oxide-nitride-oxide-silicon (SONOS) memories are widely studied as charge trapping devices for the next generation non-volatile memory [1-3]. The SONOS structure can minimize the charge leakage problem associated with conventional flash memory by using a physically discrete charge trap within the silicon nitride charge trap layer. However, SONOS devices have problems such as high erase power consumption and poor charge retention, which need to be solved before commercialization. Recently, many studies have been carried out investigating charge trapping devices and the effects of using various materials for each layer for better program/erase characteristics [4-8]. Non-stoichiometric materials such as silicon-rich silicon nitride have also been researched to obtain more suitable characteristics for memory operations [9]. In this study, multilayer structures using a lanthanum aluminum oxide charge trap instead of silicon nitride were fabricated. For the evaluation of the memory characteristics of the multilayer structures with the charge trap layer, the threshold voltage change (ΔV_{th}) during program and erase was observed using trap layers with various La/Al ratios because the energy band structure and trap level changes depend on the composition of the charge trap layer. Additionally, for low voltage operation and reduced charge leakage through the blocking oxide, an Al_2O_3 blocking oxide and Pt electrode were used [10].

*Corresponding author:
Tel : +82-2-2123-2852
Fax: +82-2-312-5375
E-mail: drchoidj@yonsei.ac.kr

Experiments

We fabricated three different ($Pt/Al_2O_3/La_xAl_yO/SiO_2/Si$) multilayer structures with different charge trap layer compositions. After a standard cleaning process for the n-type silicon (100) substrate and a native oxide removal process using a HF dipping process, the SiO_2 tunnel oxide was grown on a bare Si wafer by rapid thermal oxidation (RTO) at 850 °C in a dry O_2 atmosphere. The tunnel oxide thickness was 40 Å. For all samples, a La_xAl_yO charge trap layer with a thickness of 40 Å was deposited by metal-organic chemical vapor deposition (MOCVD), followed by deposition of a 150 Å thick Al_2O_3 blocking oxide. To deposit the charge trap layer, a tris(2,2,6,6-tetramethyl-3,5-heptanedionato) lanthanum(III) tetraglyme adduct and aluminum acetylacetonate were utilized as precursors of lanthanum and aluminum, respectively, with a N_2 carrier gas flow rate of 60 sccm. For the comparison of memory characteristics, the flow rates of each source were varied to result in La : Al flow rate ratios of 1 : 5 (10 sccm of $La(tmhd)_3$ and 50 sccm of $Al(acac)_3$), 3 : 3, and 5 : 1. At the same time, 100 sccm of O_2 was used for oxide formation. The substrate temperature was maintained at 350 °C and the working pressure was maintained at 5 torr (266.6 Pa) during deposition of all films.

Pt electrodes were deposited on the oxide multilayer by DC magnetron sputtering using a shadow mask. The thicknesses of the oxide layers were measured by ellipsometry

(Gaertner L117, $\lambda = 632.8$ nm) and the overall structure was confirmed using a high resolution transmission electron microscope (HRTEM, JEM-2100, JEOL). The compositions of the charge trapping lanthanum aluminum oxide were analyzed using X-ray photoelectron spectroscopy (XPS). The dielectric constants of lanthanum aluminum oxide were measured by a C-V analyzer (HP 4280A, 1 MHz). The memory characteristics were characterized by measuring V_{th} after a program and erase pulse. The program and erase conditions were 5-13 V for 1-1,000 ms and −5 - −13 V for 1-1,000 ms, respectively.

Results and Discussion

The dielectric constant is plotted as a function of the composition of the single layer lanthanum aluminum oxide in Fig. 1. As the La : Al ratio increased, the dielectric constant of the oxide thin film also increased. All films consisted of an amorphous phase. Pure amorphous Al_2O_3 (La : Al = 0) and pure La_2O_3 (La : Al = 1) had dielectric constants of about 7.5 and 24, respectively. When the flow rate ratios of the La source to the Al source were 1 : 5, 3 : 3, and 5 : 1, the dielectric constants were 12.4, 21.0, and 25.1, respectively.

Fig. 2 shows a HRTEM image and diffraction pattern of the fabricated $Al_2O_3/La_xAl_yO/SiO_2/Si$ structure. The trap layer within the sample shown in the image was deposited under a La source : Al source flow rate ratio of 3 : 3. From the image, the thicknesses of Al_2O_3, La_xAl_yO, and SiO_2 are 15 nm, 4 nm, and 4 nm, respectively. In addition, the entire multilayer structure is amorphous, as seen in the diffraction pattern.

The compositions of the thin films used as charge trap layers were analyzed using XPS and are shown in Table 1. As the flow rate ratio of La : Al increased, the ratio of oxygen atoms increased. The table shows that the atomic concentration of aluminum is higher than that of lanthanum in all the samples. This is due to the partial pressure difference of the La and Al sources in the carrier gas originating from the difference in molecular weights of the metal-organic sources used for deposition of each element. Also, a difference in the rates of decomposition of each source at the deposition temperature of 350 °C may also contribute to this composition inequality.

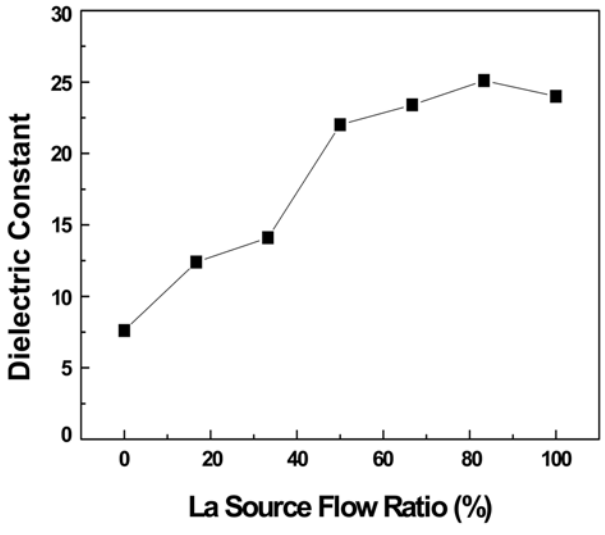

Fig. 1. The dielectric constants of lanthanum aluminum oxides with various compositions.

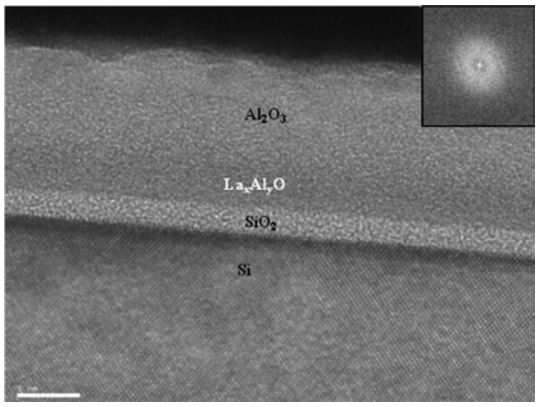

Fig. 2. HRTEM image of the $Al_2O_3/La_xAl_yO/SiO_2/Si$ structure and its diffraction pattern.

Table 1. Composition of Charge Trap Layers Analyzed by XPS with Various Flow Rate Ratios

		Source Flow Rate Ratio (La : Al)		
		1 : 5	3 : 3	5 : 1
Atomic Concentration (%)	La	5.82	10.15	13.94
	Al	34.80	29.08	24.34
	O	59.38	60.77	61.73

Fig. 3 shows the threshold voltage shift resulting from the program operation with the various compositions of the charge trap layers. In the case of the charge trap layer deposited with the La source : Al source flow rate ratio of 3 : 3, the largest threshold voltage shift with a maximum of 3.63 V was recorded after a program pulse of 11 V for 100 ms. The 5 : 1 trap layer had a ΔV_{th} of 3.38 V after a program pulse of 13 V for 100 ms, which is less than that of the 3 : 3 trap layer. The sample with the 1 : 5 trap layer showed only a ΔV_{th} of 2.22 V, which is the smallest among all samples.

The memory window values after the erase operation are shown in Fig. 4. In the case of La:Al source flow rate ratios of 1 : 5, 3 : 3, and 5 : 1, the maximum memory windows were 1.43 V, 3.49 V, and 3.01 V, respectively. The 3 : 3 trap layer sample showed the highest value while 1 : 5 trap layer sample exhibited the smallest shift, which is similar to the behavior observed in the program operation.

There are three possible explanations for these results. The first is a change of the dielectric constant in the charge trap layer. The tunneling probability of an electron in the program operation is affected by the electric field across

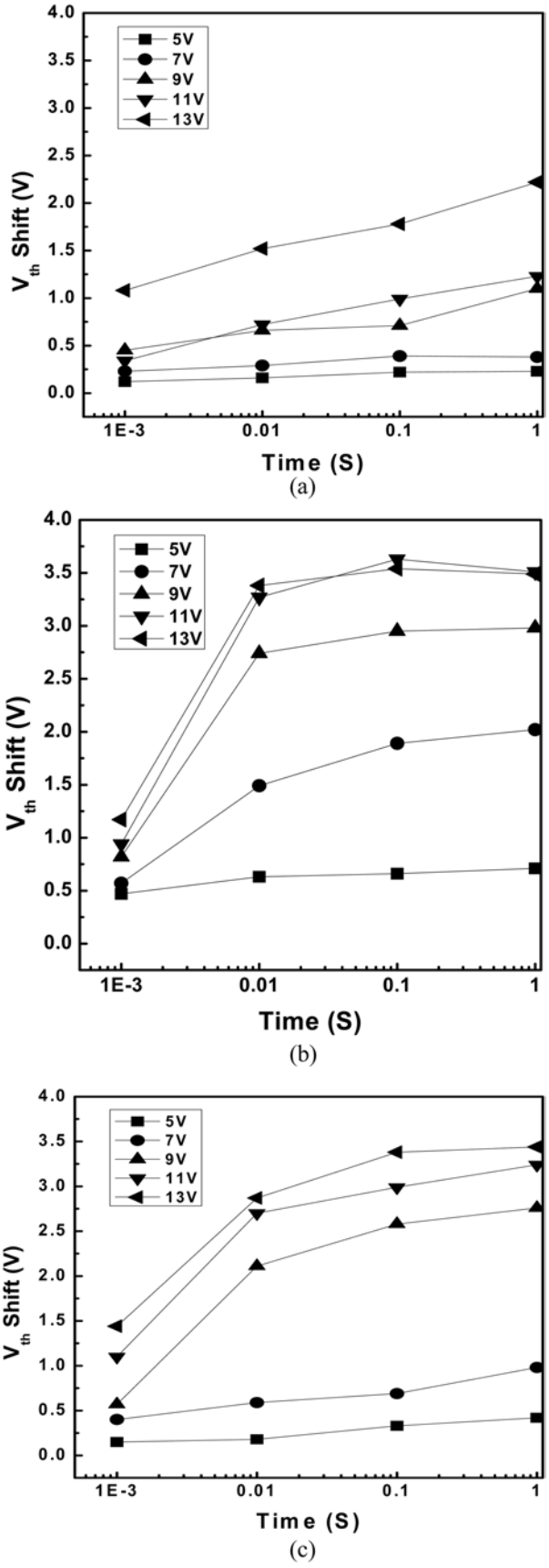

Fig. 3. Threshold voltage (V_{th}) shifts of the multilayer structures with trap layer flow rate ratios (La source:Al source) of (a) 1 : 5, (b) 3 : 3, and (c) 5 : 1 after program pulses of 5-13 V for 1-1,000 ms.

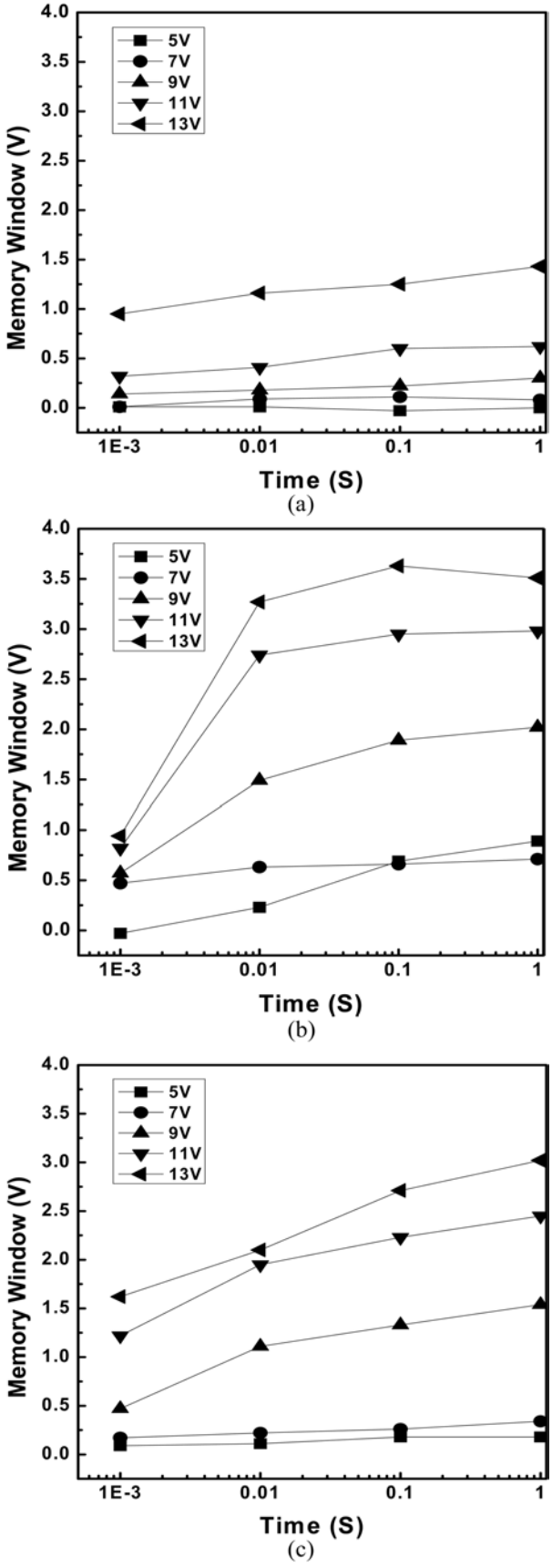

Fig. 4. Memory windows of multilayer structures with charge trap layer flow rate ratios (La source:Al source) of (a) 1 : 5, (b) 3 : 3, and (c) 5 : 1 after erase pulses of −5 - −13 V for 1-1,000 ms.

the tunnel oxide [11]. The voltage applied through the

$$V_{tunnel}=\left(\frac{\varepsilon_{to}t_{to}}{\varepsilon_{to}t_{to}+\varepsilon_{ct}t_{ct}+\varepsilon_{bo}t_{bo}}\right)V_{program} \quad (1)$$

Here, ε is the dielectric constant, t is the thickness of each layer, to denotes the tunnel oxide, ct represents the charge trap layer, bo refers to the blocking oxide, and $V_{program}$ is the total voltage across the multilayer structure in the program operation. When $V_{program}$ is 13 V, for example, a V_{tunnel} of 3.7 V is applied across the tunnel oxide within the 1 : 5 trap layer sample, while a V_{tunnel} of 5.1 V is applied across the tunnel oxide in the 5 : 1 trap layer sample. Hence, the larger La/Al ratio in the charge trap layer is, the higher the applied voltage across the tunnel oxide is for the same $V_{program}$, which leads to a more efficient program/erase operation. The second explanation for the observed behavior is that changes in the band structure of the material occur with the different compositions. Among Al_2O_3, La_2O_3, and $LaAlO_3$, the conduction band edge is the highest in Al_2O_3 and the lowest in $LaAlO_3$ [12]. Hence, when the charge trap layer contains a very high Al concentration, the program operation does not occur easily compared to with La_2O_3 or $LaAlO_3$ due to the lower tunneling probability. This explains the smallest threshold voltage shift in the sample with the La : Al = 1 : 5 charge trap. Finally, the third reason involves the change in the trap level and density of the material with different compositions. When an oxide is used as a charge trap, the oxygen vacancies act as major trap sites. In lanthanum aluminum oxide, the energy levels of oxygen vacancies from the conduction band edge are shallower than in the cases of lanthanum oxide and aluminum oxide, which leads to easier escape of electrons from the charge trap to the substrate in the erase operation [13, 14]. In addition, lanthanum aluminum oxide has additional traps originating from the ionic size difference between La^{3+} and Al^{3+}. Comparing the samples with a 5 : 1 charge trap and a 3 : 3 charge trap, the 3 : 3 charge trap sample has more oxygen vacancies originating from its lower oxygen content, while the 5 : 1 charge trap sample has more La_{Al} sites. However, the La_{Al} sites contribute much less to the memory window than oxygen vacancies since those substitutional sites are at an energetically deep trap level while oxygen vacancy sites are shallow enough to pull the charge out in the erase operation. This explains the smaller memory window of the 5 : 1 charge trap sample than that of the 3 : 3 charge trap sample. In the case of the 1 : 5 charge trap sample, the smaller initial V_{th} shift in the program operation limited the memory window. Furthermore, the trap level in aluminum oxide is known to be deep and could make the erase properties worse [15].

Fig. 5 shows the reliability of the memory characteristics after repetition of the program/erase operations. To assess reliability, the program condition was 11 V for 100 ms and the erase condition was 13 V for 100 ms. All three samples stably sustained their initial memory window for 10^4 cycles.

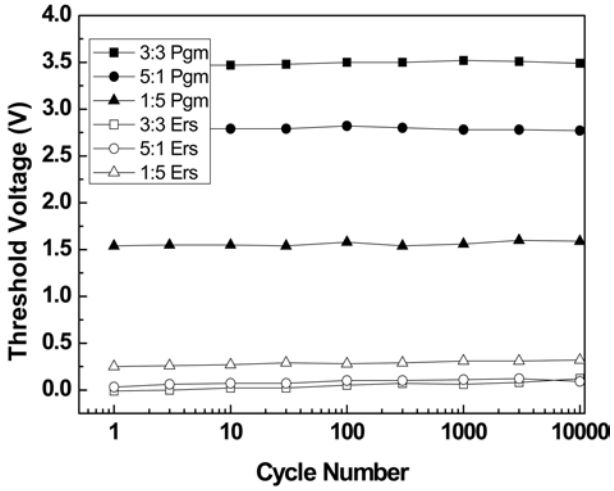

Fig. 5. Threshold voltage changes of $Pt/Al_2O_3/La_xAl_yO/SiO_2/Si$ capacitors after program/erase cycling testing.

From this result, the devices are expected to endure 10^5 program/erase cycles without a problem, which is the number of write/erase cycles suggested by the International Technology Roadmap for Semiconductor (ITRS) for a non-volatile memory [16].

Conclusions

In this study, the memory characteristics of a multilayer structure with lanthanum aluminum oxide as a charge trap layer were evaluated. Non-stoichiometric charge trap layers with three different compositions resulting from varying the La and Al source flow rate ratio in the MOCVD process were fabricated. All films fabricated by the experiments remained in an amorphous state which helped to prevent charge loss through the nonexistant grain boundaries. During evaluations of memory characteristics, the sample with a La source:Al source flow rate ratio of 3 : 3, which has a composition of 10.15% La, 29.08% Al, and 60.77% O, showed the best properties with a ΔV_{th} of 3.63 V in the program operation and a 3.48 V memory window in the erase operation. The memory properties were affected by the band structure, the trap energy level/density, and the dielectric constant of the charge trap layer. For all specimens, the initial memory windows were maintained for 10^4 cycles of the program/erase pulses, demonstrating very high reliability for next generation non-volatile memory.

Acknowledgements

This work was supported by the Second Stage of Brain Korea 21 Project in 2010.

References

1. K.N. Kim and S.Y. Lee, Microelectron. Eng. 84[9-10] (2007) 1976-1981.
2. G.W. Burr, B.N. Kurdi, J.C. Scott, C.H. Lam, K.

Gopalakrishnan and R.S. Shenoy, IBM J. Res. Dev. 52 4] (2008) 449-464.
3. H.M. White and A.D. Adams, J. Bu, IEEE Circuits Devices, 16[4] (2000) 22-31.
4. J.A. Felix, J.R. Schwank, D.M. Fleetwood, M.R. Shaneyfelt and E.P. Gusev, Microelectron. Reliab. 44[4] (2004) 563-575.
5. T.M. Pan and T.Y. Yu, Appl. Phys. Lett. 92 (2008) 112906-1-112906-3.
6. Y.N. Tan, W.K. Chim, B.J. Cho, and W.K. Choi, IEEE T. Electron Dev. 51[7] (2004) 1143-1147.
7. S.H. Lin, H.J. Yang, W.B. Chen, F.S. Yeh, S.P. McAlister and A. Chin, IEEE T. Electron Dev. 55[7] (2008) 1708-1713.
8. J.M. Kang, K.H. Keem, D.Y. Jeong, M.Y. Park, D.M. Whang and S.S. Kim, J. Mater. Sci. 43[10] (2008) 3424-3428.
9. T.H. Kim, I.H. Park, J.D. Lee, H.C. Shin and B. G. Park, Appl. Phys. Lett. 89 (2006) 063508-1-063508-3.
10. S. Jeon, J.H. Han, J.H. Lee, S. Choi, H. Hwang and C. Kim, IEEE T. Electron Dev. 52[12] (2005) 2654-2659.
11. C.M. Compagnoni, A. Mauri, S.M. Amoroso, A. Maconi and A.S. Spinelli, IEEE T. Electron Dev. 56[9] (2009) 2008-2015.
12. G. D. Wilk, R. M. Wallace, J. M. Anthony, J. Appl. Phys. 89 (2001) 5243-5275.
13. K. Xiong, J. Robertson and S.J. Clark, Appl. Phys. Lett. 89 (2006) 022907-1-022907-3.
14. B. Sen, H. Wong, J. Molina, H. Iwai, J.A. Ng, K. Kakushima and C.K. Sarkar, Solid State Electron., 51[3] (2007) 475-480.
15. T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi and H. Tanaka, Symposium on VLSl Technology Digest of Technical Papers (2003) p. 27-28.
16. International Technology Roadmap for Semiconductors, 2008 Update.