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Electrical characteristics of $Al_2O_3/Ta_2O_5/SiO_2$ multi-layer films using various tunnel oxide thicknesses at different annealing temperatures

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In this study, we investigated the electrical properties of $Al_2O_3/Ta_2O_5/SiO_2$ (ATS) films using various tunnel oxide (bottom oxide) thicknesses at different annealing temperatures. With a 5 nm thick tunnel oxide, the program/erase conditions were 11 V for 100 ms and −13 V for 100 ms, respectively. The memory window of the film was 0.91 V. To improve the film quality, the film was annealed at 900 °C. The thickness of the multi-layer film decreased after the annealing process. The program/erase conditions of the annealed films changed to 9 V for 100 ms and −13 V for 100 ms, respectively. The memory window of the annealed film was 1.05 V. The retention properties of the as-deposited and annealed films did not change up to 10^4 cycles. The electrical characteristics of ATS structures using various tunnel oxide thicknesses at different annealing temperatures were investigated for application in next generation non-volatile memories.

Key words: Ta_2O_5, high-k, MOCVD, retention, annealing.

Introduction

Recently, the market for NAND (Not AND) flash memory has gradually expanded due to increased usage of portable storage devices and notebooks. Currently, a NAND flash memory uses a floating gate to store charge carriers. However, the use of a floating gate causes several serious problems. First, as the dimension between the cells of the flash memory decreases, the dimension between the floating gates decreases [1]. Therefore, the working cell is interfered with by other working cells during the program/erase operation. Secondly, the stored charges can easily move out of the programmed cell due to charge leakage through the grain boundaries [2] causing the retention characteristics of the flash memory to become worse. To solve these problems, SONOS and MONOS (silicon/metal-oxide-nitride-oxide-silicon) structures have been suggested instead of using floating gates [3-5]. However, these structures also have limitations. The 2008 ITRS data forecast that the thicknesses of the blocking oxide (top oxide), charge trap layer (CTL), and tunnel oxide (bottom oxide) will be 8 nm, 7 nm, and 4 nm (maximum thicknesses), respectively, until 2010 [6].

The SONOS and MONOS structures usually use SiO_2 as the tunnel oxide. As the thickness of the SiO_2 decreases, the stress-induced leakage current (SILC) characteristics and the retention characteristics continuously degrade [7]. Hence, the thickness of the tunnel oxide needs to be optimized.

The CTL and blocking oxide should be replaced by a high-k material to improve the erase speed and the retention characteristics. Since high-k materials have relatively high dielectric constants compared to Si_3N_4, the applied electric field decreases during the program/erase operation [8]. Tan *et al*. and Wang *et al.* proposed $Hf_xAl_yO_z$ and Ta_2O_5 as CTL materials and reported improved retention and endurance characteristics [9-10].

SONOS and MONOS structures using SiO_2 as a blocking oxide have attracted the interest of many research groups. As the thickness of the blocking oxide continuously decreases, the problems of increasing erase speed and high operation voltages become more common. Since the extra charges are injected into the CTL through defect sites of the blocking oxide during the applied voltage, the erase time increases. Since the applied electric field also decreases at the tunnel oxide with reduced blocking oxide thickness, the program and erase operations are at a relatively high voltage. Hence, the use of high-k material prevents electron back tunneling (EBT) and a relatively low operation voltage is possible [11].

In order to investigate the memory characteristics of $Al_2O_3/Ta_2O_5/SiO_2$ (ATS) multi-layer films, we used Al_2O_3 as the top oxide, Ta_2O_5 as the CTL, and SiO_2 as the bottom oxide. We also investigated the retention characteristics with various tunnel oxide thicknesses to optimize the film thickness. The films were then annealed at 900 °C and the changes of the electrical properties of the annealed films were investigated.

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Experimental

The ATS multilayer films were deposited on (100) n-type Si wafers (SILTRON, Korea) using the metal organic chemical vapor deposition (MOCVD) method. The thicknesses of the tunnel oxide (bottom oxide) based on 2008 ITRS data were 3 nm, 4 nm, and 5 nm. The thicknesses of the blocking oxide (top oxide) and charge trap layer (CTL) were 10.5 nm and 7.2 nm, respectively.

Tantalum tetraethoxy acetylacetonate [$Ta(OC_2H_5)_4(CH_3COCHCOCH_3)$, Stream Chemical Inc., USA] and Al-acetylacetonate [$Al(CH_3COCH_3)_3$, Stream Chemical Inc., USA] were used as the Ta and Al metal precursors, respectively. N_2 was used as the carrier gas for the Ta and Al precursors. Before deposition, the native oxide layer on the Si wafer was removed using 10% dilute hydrofluoric acid (DHF). The tunnel oxide (SiO_2) was formed by thermal oxidation using the rapid thermal process (RTP, ULVAC MILA 3000). In order to form tunnel oxide thicknesses of 3 nm, 4 nm, and 5 nm, we oxidized the Si substrate for 5 minutes, 10 minutes, and 15 minutes at 850 °C, respectively. The deposition temperature of Ta_2O_5 (CTL) and Al_2O_3 (top oxide) was 200 °C under a pressure of 5 torr (266.6 Pa). The thicknesses of the Ta_2O_5 (CTL) and Al_2O_3 layers were 7.2 nm and 10.5 nm, respectively. Since the grain boundaries of the crystalline phase become a path for leakage current, we confirmed the amorphous phase of each layer deposited at 200 °C using X-ray diffraction (XRD). The film thicknesses were measured by an ellipsometer (Gartner, L117, $\lambda = 632.8$ nm). A Pt electrode was deposited using magnetron sputtering with a shadow mask. The capacitor area was $9.25 \times 10\ cm^2$. After fabrication of the ($Pt/Al_2O_3/Ta_2O_5/SiO_2/Si$) capacitors, the specimen was annealed by RTP at 900 °C.

We measured the dielectric constant, the memory window, and the retention characteristics using a capacitance-voltage (C-V) analyzer (Keithley 590) at a frequency of 1 MHz. We measured the I-V characteristics using a HP 4145B. We used high resolution transmission electron microscopy (HRTEM, Tecnai G2 F20 S-Twin) to confirm the interfacial layer.

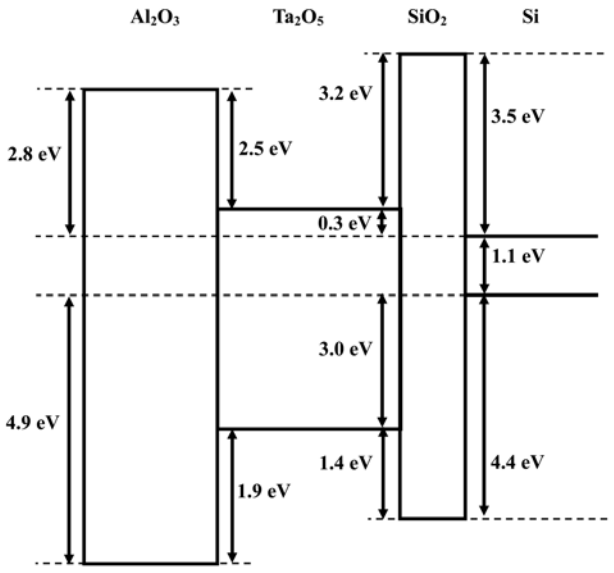

Fig. 1. The band diagram of the $Al_2O_3/Ta_2O_5/SiO_2$ (ATS) films.

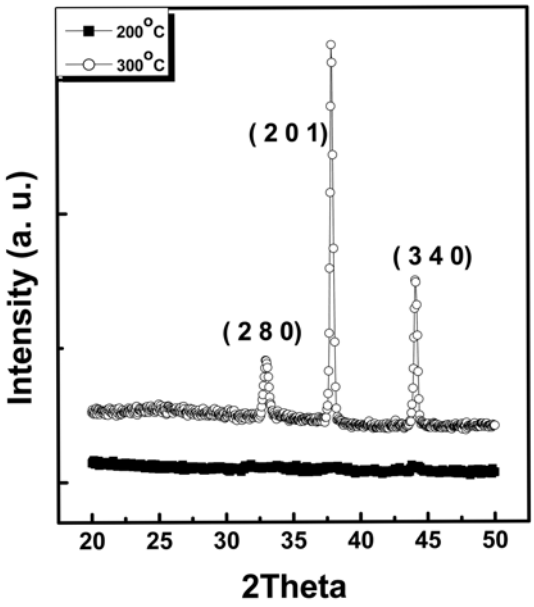

Fig. 2. The XRD peaks of a Ta_2O_5 single layer at 200 °C and 300 °C.

Results and Discussion

Fig. 1 shows the energy band diagram of the $Al_2O_3/Ta_2O_5/SiO_2$ (ATS) multi-layer film [12]. The conduction band offsets of Al_2O_3, Ta_2O_5, and SiO_2 were 2.8 eV, 0.3 eV, and 3.5 eV, respectively. The difference of the conduction band offset between the CTL (Ta_2O_5) and tunnel oxide (SiO_2) is 3.2 eV. The difference of the conduction band offset of Ta_2O_5/SiO_2 is deeper than that of Si_3N_4/SiO_2 (1.1 eV) in SONOS structures [12]. Therefore, the large difference of the conduction offset of Ta_2O_5/SiO_2 is expected to easily allow storage compared to SONOS structures [8]. According to 2008 ITRS data, the blocking oxide thickness will be 8 nm until 2015. With a SiO_2 ($\varepsilon = 3.9$) thickness as the blocking oxide of 8 nm, electron back tunneling (EBT) can not be prevented. Since the electrical thickness of Al_2O_3 is higher than that of SiO_2 at the same physical thickness to prevent EBT, we used Al_2O_3 ($\varepsilon = 9$) as a blocking oxide [12].

Fig. 2 shows the XRD data of a Ta_2O_5 single layer. Kukli *et al*. reported that Ta_2O_5 films have orthorhombic β structures when the deposition temperature is higher than 350 °C [13]. The orthorhombic β structures also have oxygen vacancies and these vacancies could become a leakage current path [13-15]. Hence, the Ta_2O_5 films should be deposited at temperatures below 350 °C. Ta_2O_5 films have pseudo hexagonal structures below 350 °C [13-14]. Asghar *et al*. reported that Ta_2O_5 was crystallized at substrate temperatures slightly higher than 200 °C [16]. Since electrons easily move out through grain boundaries in the case of crystallized CTL, the retention characteristics degrade.

Hence, we deposited the Ta_2O_5 films on Si (100) substrates at 200 °C and 300 °C to confirm the crystalline phase. In Fig. 2, we observed an amorphous phase at a deposition temperature of 200 °C. At a deposition temperature of 300 °C, the Ta_2O_5 film became crystallized. We did not deposit a Ta_2O_5 film at 150 °C.

Fig. 3(a) shows the TEM image of a $Al_2O_3/Ta_2O_5/SiO_2$ (ATS) film with a 5 nm thick tunnel oxide. The ATS films showed an amorphous structure. The thicknesses of the Al_2O_3, Ta_2O_5, and SiO_2 layers were 10.5 nm, 7.2 nm, and 5 nm, respectively. In the TEM image, an interfacial layer of Si_xO_y with a thickness of 4.4 Å was also formed between the Si substrate and the SiO_2 layer.

Fig. 3(b) shows the C-V characteristics of the tunnel oxides with thicknesses of 3 nm, 4 nm, and 5 nm. The sweep voltage was varied from −3 V to 3 V. To remove the charge remaining in the ATS films before the program/erase operation, a full erase operation was performed. The condition of full erase was −13 V for 100 ms. The applied voltages of the program/erase operation ranged from 7 V to 13 V (for 3-1,000 ms) and from −7 V to −13 V (for 3-1,000 ms), respectively. The program/erase conditions of the ATS film using the 3 nm tunnel oxide were 9 V for 10 ms and −11 V for 100 ms, and the memory window was about 0.51 V. On the other hand, the results of the ATS films using 4 nm and 5 nm thick tunnel oxides were 11 V for 10 ms (program)/−11 V for 100 ms (erase) and 11 V for 100 ms (program)/−11 V for 100 ms (erase), respectively. The memory windows of the ATS films were 0.78 V and 0.91 V with tunnel oxide thicknesses of 4 nm and 5 nm, respectively. From this result, the memory window depends on the thickness of the tunnel oxide. Since the tunnel oxide thicknesses were very thin, charge loss can be easily caused by defects in the tunnel oxide (SiO_2). To change the threshold voltage, the program time of the ATS film using the 5 nm thick tunnel oxide increased. However, the memory window of the ATS film using the 5 nm thick tunnel oxide was higher than the ATS film using the 4 nm thick tunnel oxide. Hence, the optimal thickness of the tunnel oxide (SiO_2) in this study was 5 nm.

Fig. 3(c) shows the retention characteristics over 10^4 cycles with ATS film tunnel oxide thicknesses of 3 nm, 4 nm, and 5 nm. The memory windows of the ATS films with tunnel oxide thicknesses of 3 nm, 4 nm, and 5 nm were 0.41 V, 0.66 V, and 0.81 V, respectively, after 10^4 cycles. The memory windows after 10^4 cycles degraded by 20%, 16%, and 11%, compared to their initial memory windows, with tunnel oxide thicknesses of 3 nm, 4 nm, and 5 nm, respectively. Usually, the Fowler-Nordheim (F-N) electron tunneling phenomenon is used during program/erase operations. The F-N tunneling is quantum-mechanical tunneling induced by an electric field. When a large electric field is applied to a device, it enables the electrons to tunnel [17]. However, the electrons result in physical stress in the tunnel oxide due to the electron mass [18]. Therefore, the retention characteristics degrade. In general, the memory window is reduced by 60% of its initial memory window over 10 years

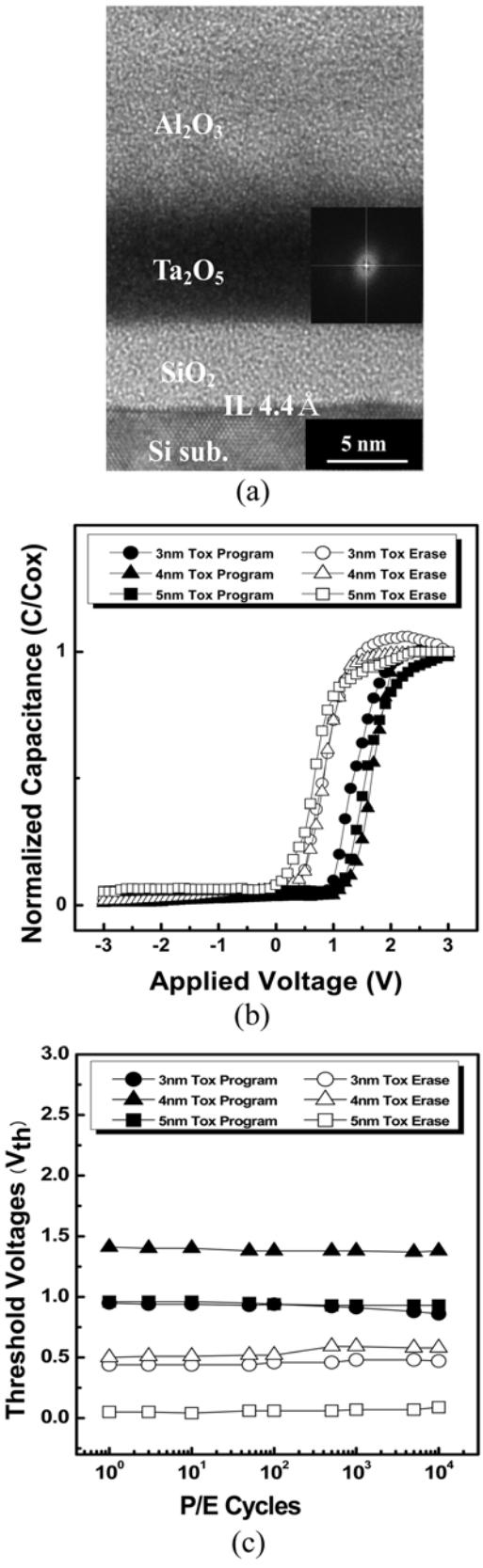

Fig. 3. (a) HR-TEM image of the ATS structure with a 5 nm thick tunnel oxide layer deposited on a Si (100) substrate at 200 °C, (b) C-V characteristics, and (c) retention characteristics of the ATS multi-layered structures with 3 nm, 4 nm, and 5 nm thick tunnel oxide layers.

(about 10^8 cycles) [18]. In the ATS film with the 5 nm thick tunnel oxide, the memory windows decreased from 0.91 V (first cycle) to 0.81 V (after 10^4 cycles). By linearly fitting the retention characteristic over 10^4 cycles, the memory window is predicted to degrade by 50% after 10^7 cycles. Hence, the ATS film with a 5 nm thick tunnel oxide is a promising candidate for memory applications. In this study, the memory window and the retention characteristic were good when the thickness of the tunnel oxide was 5 nm.

Fig. 4(a) shows a TEM image of the ATS film with a 5 nm thick tunnel oxide annealed at 900 °C. After the annealing process, the thicknesses of the Al_2O_3, Ta_2O_5, and SiO_2 layers decreased from 10.5 nm, 7.2 nm, and 5 nm to 9.5 nm, 6.4 nm, and 4.4 nm, respectively, as shown in the TEM image. The interfacial layer between the Si substrate and the SiO_2 layer also grew by about 9.4 Å. According to a report by Jun *et al*., the interfacial layer grows by the rapid diffusion of residual oxygen on the surface of the Si substrate during the annealing process [19]. It was reported that Ta_2O_5 single layers became crystallized at 800 °C when the thickness of the Ta_2O_5 layer was about 400 nm [20]. However, in this study, the Ta_2O_5 structures showed an amorphous structure after annealing at 900 °C. According to Jun *et al*. [21], thin films of about 10 nm were not crystallized at 900 °C. One of the reasons for this behavior is that the nucleation barrier height is high due to surface and interface energy. If the thickness of the film is similar to the dimension of a nucleus, it is hard for the film to nucleate and crystallize [21, 22]. Since the Ta_2O_5 thickness was thin (7 nm), the Ta_2O_5 structures were amorphous after annealing at 900 °C.

Fig. 4(b) shows the C-V characteristics of fully erased, programmed, and erased ATS films with a 5 nm thick tunnel oxide annealed at 900 °C. The program/erase conditions of the annealed ATS films were 9 V and −11 V for 100 ms. The memory window was 1.05 V. Therefore, the program conditions of the ATS film with a 5 nm thick tunnel oxide decreased from 11 V to 9 V for 100 ms following annealing. Since the thickness of the ATS films with a 5 nm thick tunnel oxide was reduced after the annealing process, the program voltage decreased. In particular, the thin tunnel oxide easily induces electron tunneling. On the other hand, the memory windows of the as-deposited and annealed ATS films did not change significantly. This phenomenon is caused by the interfacial layer (SiO_2/Si) of the film. Since the interfacial layer was not dense, the electrons could be easily trapped [23-24].

Fig. 4(c) shows the retention characteristic of the ATS film after annealing at 900 °C. The memory window of the annealed ATS film was 0.95 V after 10^4 cycles. The memory window of the annealed ATS film after 10^4 cycles degraded by 9.5% compared to the memory window after the first cycle. The retention degradations of the as-deposited and annealed films with a 5 nm thick tunnel oxide did not change greatly after 10^4 program/erase cycles. In Fig. 3(b), we hypothesized that the reason for this was the thickness reduction and the interfacial layer. Since the interfacial layer

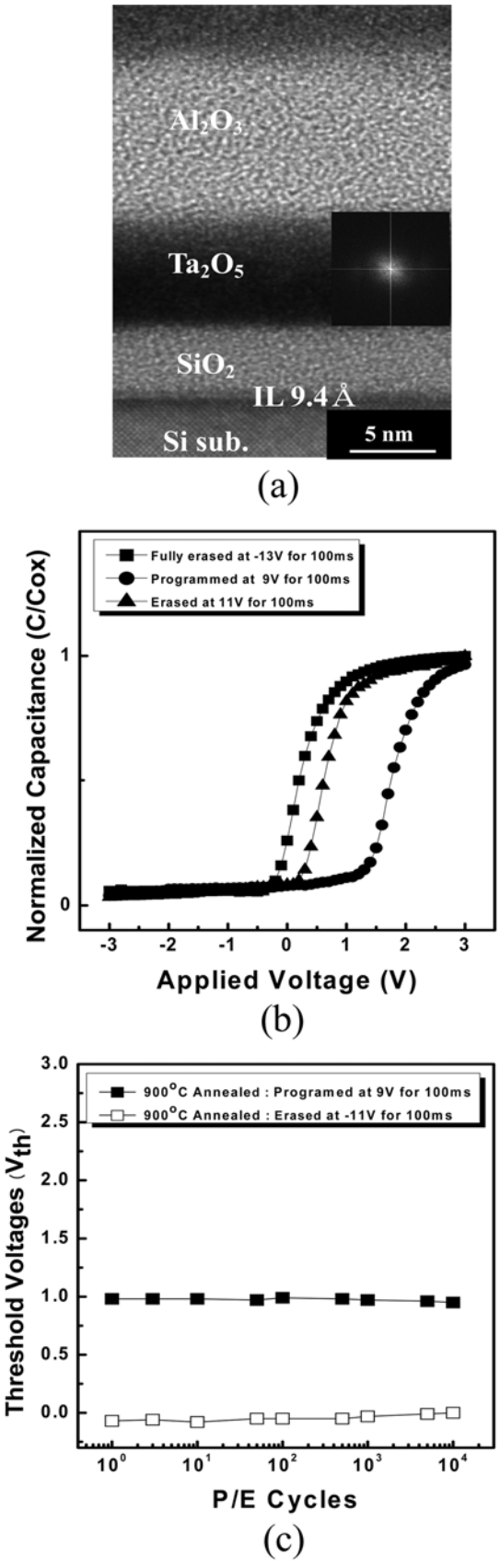

Fig. 4. (a) HR-TEM image of the ATS structure, (b) C-V characteristics, and (c) retention characteristics of the ATS multi-layered structure with a 5 nm thick tunnel oxide after annealing at 900 °C.

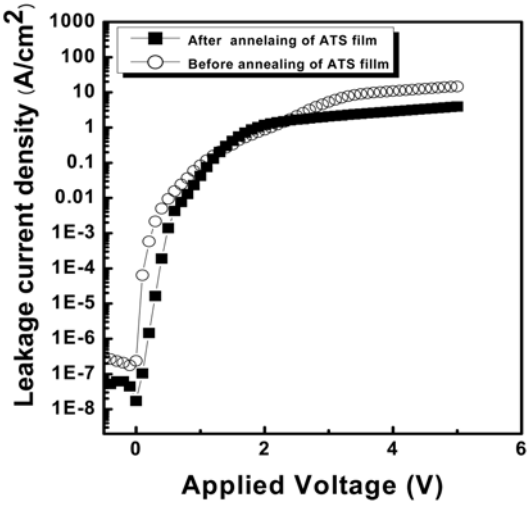

Fig. 5. Leakage current densities as a function of the applied voltage of as-deposited and annealed ATS structures with a 5 nm thick tunnel oxide layer.

has many defects, the electrons could be easily trapped. Hence, ATS structures became a low power device through the annealing process.

Fig. 5 shows the leakage current densities of the ATS films with a 5 nm thick tunnel oxide. The operation voltage of the latest flash memory is under 3 V. Hence, we measured the leakage current densities of ATS films with a 5 nm thick tunnel oxide from 0 V to 5 V. The leakage current densities of the as-deposited and annealed ATS films with a 5 nm thick tunnel oxide were 4.2×10^{-2} A/cm^2 and 8.5×10^{-2} A/cm^2 at 1 V, respectively. The SILC value increased due to the reduction of the thicknesses of the ATS layers with a 5 nm thick tunnel oxide. According to 2007 ITRS data, leakage current densities of a flash memory are below 10^{-1} A/cm^2 at 1 V for memory operation [25]. Hence, the annealed ATS films can be used as a flash memory.

Conclusions

We quantified the memory window and retention characteristic as the thickness of the tunnel oxide was varied from 3 nm, to 4 nm, and 5 nm. The thicknesses of the Al_2O_3 and Ta_2O_5 layers of the ATS film were 10.5 nm and 7.2 nm, respectively. The memory window (0.91 V for 100 ms) of the ATS ($Al_2O_3/Ta_2O_5/SiO_2$) film with a 5 nm thick tunnel oxide was the best. The memory window degraded by 11% to 0.81 V after 10^4 cycles. After annealing the ATS film with a 5 nm thick tunnel oxide at 900 °C, the thicknesses of the Al_2O_3, Ta_2O_5, and SiO_2 layers decreased to 4.4 nm, 6.4 nm, and 9.5 nm, respectively. An interfacial layer with a thickness of 9.4 Å also formed between the Si substrate and the SiO_2 layer. The program voltage of the annealed ATS film decreased due to the thickness reduction and an interfacial layer. The memory window of the annealed ATS film decreased from 1.05 V to 0.95 V after 10^4 cycles. The leakage current densities were also of the order of 10^{-2} A/cm^2 at 1 V. In conclusion, the use of annealed ATS films is possible. Hence, the ATS film with a 5 nm thick tunnel oxide can be used as a next generation flash memory.

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