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Electrical behavior of ultra-thin body silicon-on-insulator n-MOSFETs at a high operating temperature

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Recessed ultra-thin body (UTB) silicon-on-insulator (SOI) n-meta-oxide-semiconductor field-effect transistors (MOSFETs) with a top silicon thickness of less than 10 nm were successfully fabricated. We investigated the dependence of their electrical characteristics, such as subthreshold conduction and effective mobility, on the operating temperature the different channel thicknesses of less than 10 nm. In the case of a 4.5-nm-channel UTB SOI n-MOSFET, it was observed that as the temperature rises, the subthreshold conduction characteristic became sensitive to temperature, while the leakage current was insensitive to temperature. In addition, the effective mobility of a 4.5-nm-thick UTB SOI n-MOSFET decreased because the carrier transport was suppressed by scatterings both from surface and interface roughness scatterings. In particular, we confirmed that mobility differences at the effective fields of 0.1 and 0.3 MV/cm decrease with a rise in temperature resulting from the mobility being dominated by phonon scattering rather than scatterings from surface roughness.

Key words: Recess channel, Heating, Nano-SOI, Thermal conductivity.

Introduction

As a silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistor (MOSFET) requires high-speed and low-power applicable devices, a fully depleted (FD) SOI MOSFET, which has a thin top layer of silicon, is the most suitable device structure. Because the short channel and floating body effects are suppressed and the junction depth is restricted in the shallow thickness in a FD SOI MOSFET, which has been the focus of more research than a partially depleted (PD) SOI MOSFET [1-4]. A short channel SOI n-MOSFET below 45-nm gate length should have less than 15-nm top silicon thickness for FD-type high-performance-operation, which is called an ultra-thin body (UTB) SOI n-MOSFET [5]. However, SOI MOSFETs are prone to self-heating because the thermal conductivity of the SiO_2 layer is lower than the silicon layer [6-9].

Much research on the electrical characteristics of UTB SOI, such as the channel mobility, V_T, and other characteristics has been reported [10-12]. Here, there are two factors to consider for an analysis of the electrical characteristic for an UTB SOI n-MOSFET. The inversion-electron-channel thickness of an n-MOSFET is less than 10 nm. If the top silicon layer is thinner than the inversion layer, the channel thickness is determined by a decrease in the top silicon layer thickness. An UTB SOI n-MOSFET scatterings from suffers interfacial roughness and top silicon layer thickness fluctuations (T_{Si}) [12-13]. Moreover, in the real operation of an UTB SOI n-MOSFET, it is important to investigate the electrical characteristics of an UTB SOI n-MOSFET operating at a high temperature and with less than below 10 nm top silicon layer thickness, because the channel temperature rises by up to 350 K from the self-heating effect [10, 14].

In this paper, we demonstrate the electrical characteristics of UTB SOI n-MOSFET such as the I_D-V_D, I_D-V_G characteristics, threshold voltage (V_T), subthreshold slope (S), leakage current (I_{leak}), and effective mobility (μ_{eff}) as s function of heating. We will discuss performance degradation within increase in the operation temperature.

Experiment

An SOI wafer with a 20-nm-thick top silicon layer, 177-nm-thick BOX, and 10-Ω·cm resistivity was used as a starting substrate. Mesa-isolation processes were performed through reactive ion etching, and 20-μm width active regions were fabricated [15]. Channel regions were selectively etched and thinned channel layers of 5, 7.5, and 10 nm were fabricated. Thermal oxidation was performed for 10 minutes at 880 °C and 100-nm-thick n^+ doped poly-silicon layer was deposited by low-pressure chemical vapor deposition (LPCVD) with a $POCl_3$ atmosphere. 20-μm-length gates were defined to etch the patterned poly-silicon which was doped a with a 10^{15} cm^{-2} dose of phosphorus at 500 °C by a plasma immersion doping method to create very shallow source and drain regions [16]. Then, post-rapid thermal annealing (post-RTA) was used to enhance the interfacial property and remove the positive charges [17]. Finally, recessed

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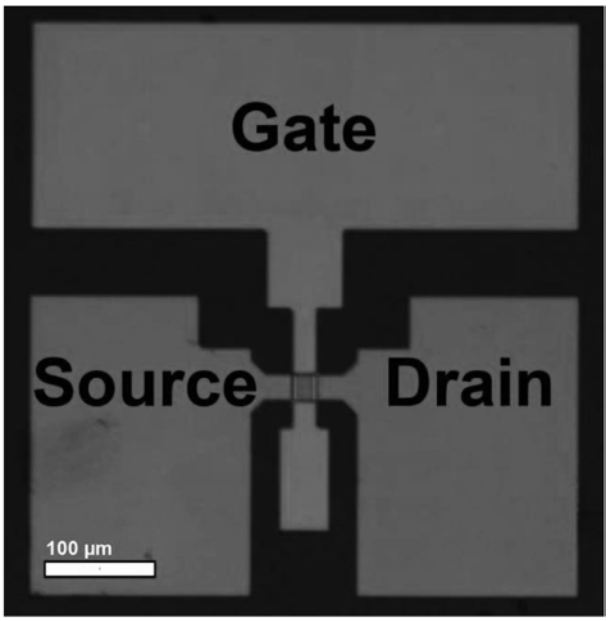

Fig. 1. Optical microscope image of an UTB SOI n-MOSFET.

channel UTB SOI n-MOSFETs were successfully fabricated and the electrical characteristics such as I_D-V_D, I_D-V_G, V_T, S, I_{leak}, and μ_{eff} were characterized.

Results and Discussion

Fig. 1 shows an optical microscope image of an UTB SOI n-MOSFET. The top silicon and gate oxide thicknesses were confirmed by transmission electron microscopy (TEM) as shown in Fig. 2. The cross sectional TEM images show that the top silicon layer thicknesses were 4.5, 7.3, and 8.5 nm, and the gate oxide thicknesses were 4.5-, 7.3- and 8.5-nm-thick SOI n-MOSFETs were 5.9, 5.3, and 5.7 nm, respectively.

Fig. 3 shows I_D-V_D curves of 4.5-, 7.3- and 8.5-nm-thick SOI n-MOSFETs as a function of operating temperature. This figure demonstrates that, as the temperature rises from 25 °C to 80 °C, the saturated drain current with a $V_G - V_T = 2$ V bias decreases 16.1% in 4.5-nm-thick, 16.8% in 7.3-nm-thick, and 19.4% in 8.5-nm-thick SOI n-MOSFETs, respectively. This implies that when the temperature rises, the thicker UTB SOI n-MOSFET's current decreased much more far the than thinner samples because the channel mobility for the thicker top silicon layer was dominated by phonon scattering rather than scattering due to the surface roughness.

In a UTB SOI n-MOSFET with the top silicon thickness of less than 6 nm, the electron mobility is governed by two dominant scattering factors: The one is surface

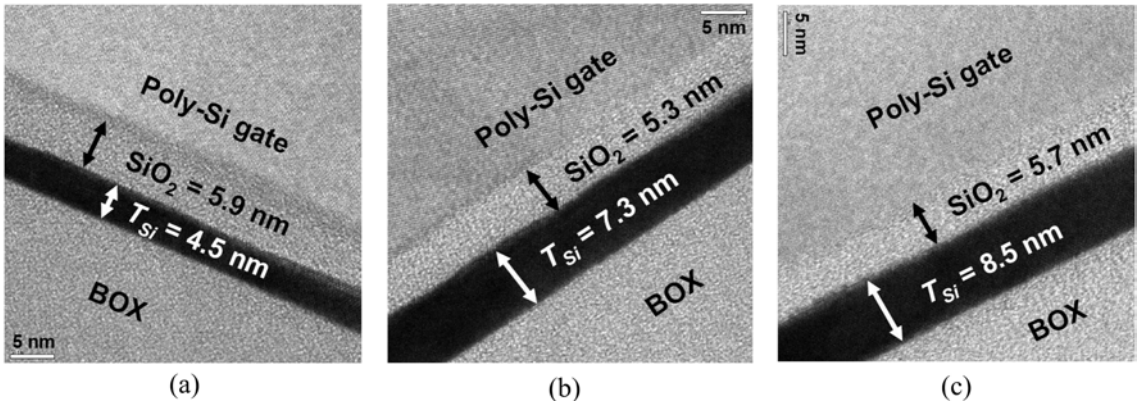

Fig. 2. TEM images of ultra-thin samples. (a) 4.5 nm, (b) 7.3 nm and (c) 8.5 nm-thick top Si SOI.

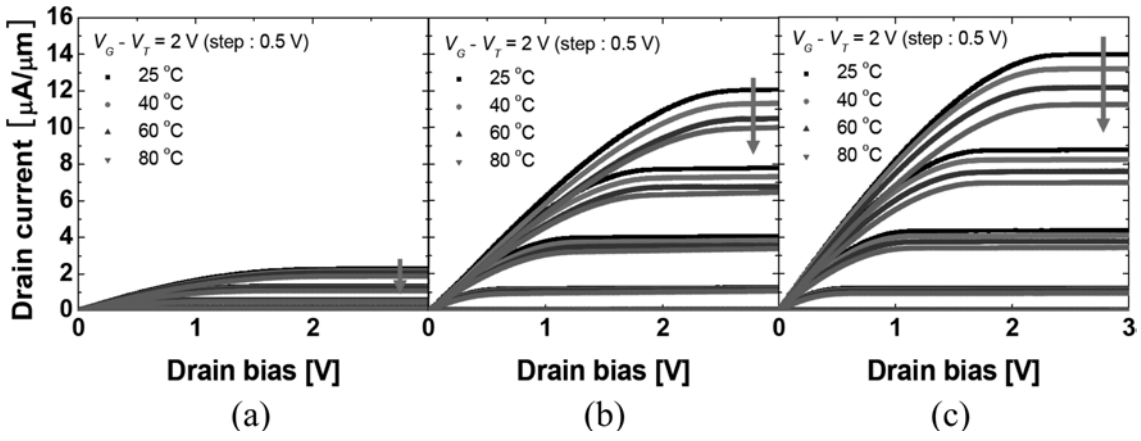

Fig. 3. I_D–V_D characteristics dependence on the operating temperature, (a) 4.5 nm (b) 7.3 nm and (c) 8.5 nm-thick top Si UTB SOI n-MOSFETs.

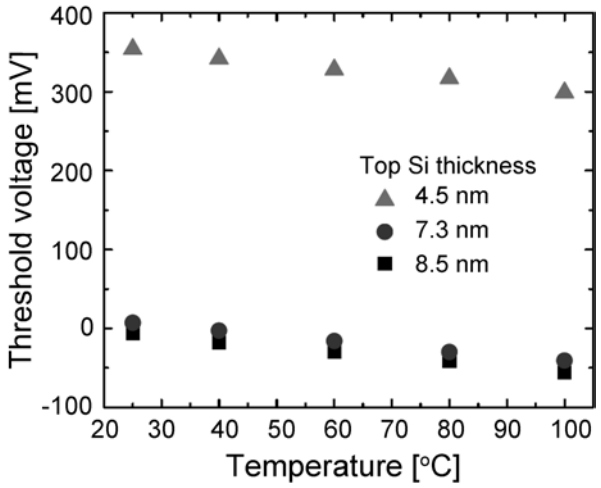

Fig. 4. Threshold voltage vs. temperature as a function of top Si layer thickness.

roughness scattering generating between the gate oxide and the top silicon, and the other is interface roughness scattering generating between the top silicon and the buried oxide layer [18].

Fig. 4 shows the V_T variation as a function of operating temperature. It was confirmed that a 4.5-nm-thick UTB SOI n-MOSFET's V_T is 350 mV higher than for the other samples. This result can probably be attributed to the following two facts. One is that, in the top silicon lager thinner than 6 nm, generating the volume inversion needs more energy because subband energies increase resulting from quantum mechanics phenomena [19]. The other is that, in the FD UTB SOI n-MOSFET, V_T decreases with an increase in the temperature because Φ_F is very sensitive to the heat [20]. The relationship between V_T and temperature can be understood from the following equation:

$$\frac{dV_T}{dT} = \frac{d\Phi_F}{dT}\left[1 + \frac{q}{C_{ox}}\sqrt{\frac{\varepsilon_{Si}N_a}{K_B T \ln\left(\frac{N_a}{n_i}\right)}}\right] \quad (1)$$

where $_F$ is potential difference between the Fermi level and the intrinsic level, C_{ox} is the oxide capacitance, ε_{Si} is the dielectric constant of silicon, N_a is the acceptor concentration, k_B is Boltzmann's constant, and n_i is the intrinsic carrier density.

Our experiment data in Fig. 4 can be also explained by Eq. (1); V_T decreased linearly with temperature regardless of the top silicon layer thickness.

Fig. 5(a) shows I_D-V_G curves and (b) shows the subthreshold slopes (S) as a function of operating temperature. These show that the subthreshold conduction characteristics of UTB SOI n-MOSFETs are vary with the operating temperature. It was observed that the tendency of the S value increases with the temperature, as shown in Fig. 5(a) and (b). Fig. 5(b) shows S values

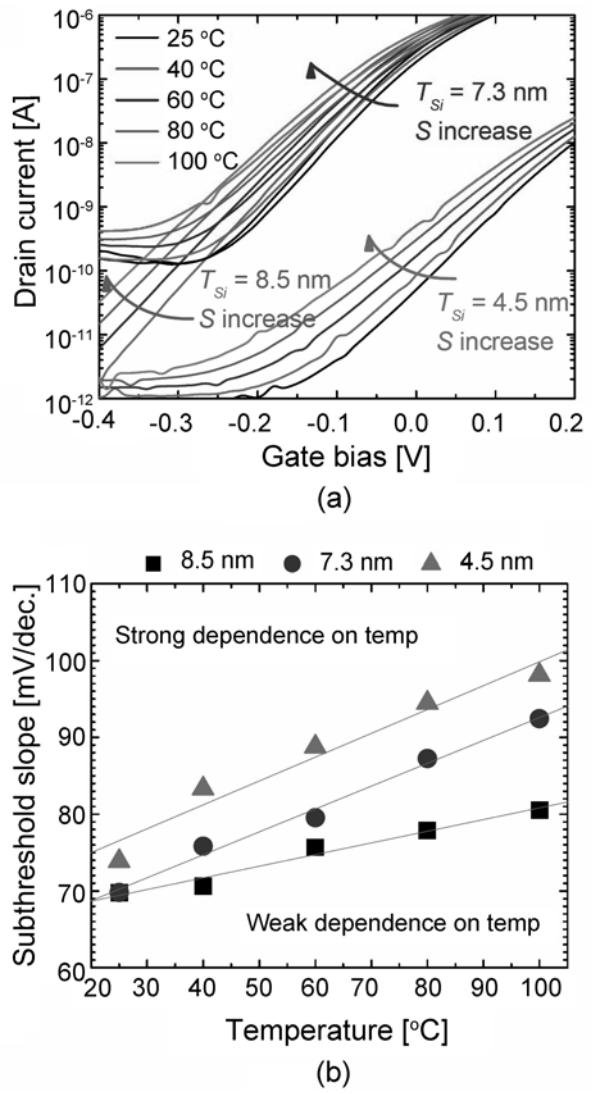

Fig. 5. Subthreshold conduction characteristics, (a) I_D–V_G curves and (b) slopes as a function of operating temperature.

with different silicon layer thicknesses. It implies that the thinner UTB SOI n-MOSFET's S values are more sensitive to the temperature than thicker ones. In other words, the S value of a 4.5-nm-thick UTB SOI n-MOSFET increases with a slope of 311 μVdec.$^{-1}$°C^{-1}. This is about two times steeper than the 8.5-nm-thick UTB SOI n-MOSFET's slope, 152 μVdec.$^{-1}$°C^{-1}. This can be explained by the fact that the depletion capacitance in the channel of a thinner thick UTB SOI n-MOSFET is larger than thicker thick one, which makes electrons conduct easily in the weak inversion state, resulting in an increase in the slope of S along with the temperature.

Fig. 6 shows the leakage current characteristics in the operating temperature range of 25 °C to 100 °C. The leakage current of an n-MOSFET at room temperature was normalized. This figure shows that the leakage current for all samples increases with the temperature. In particular, Fig. 6 demonstrate that the leakage current in the 8.5-nm-thick UTB SOI n-MOSFET was

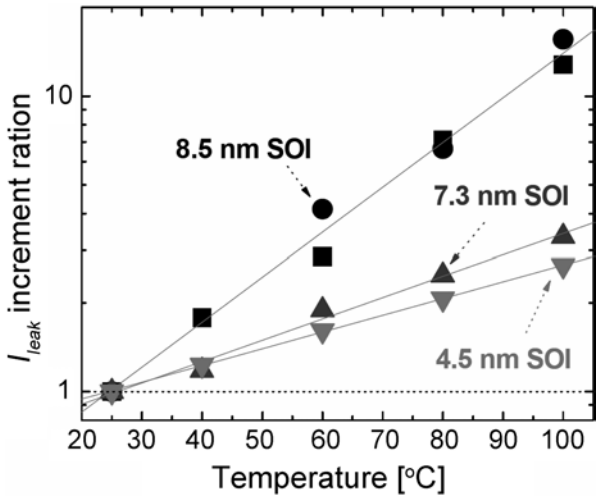

Fig. 6. Leakage current increment ratio vs. operating temperature.

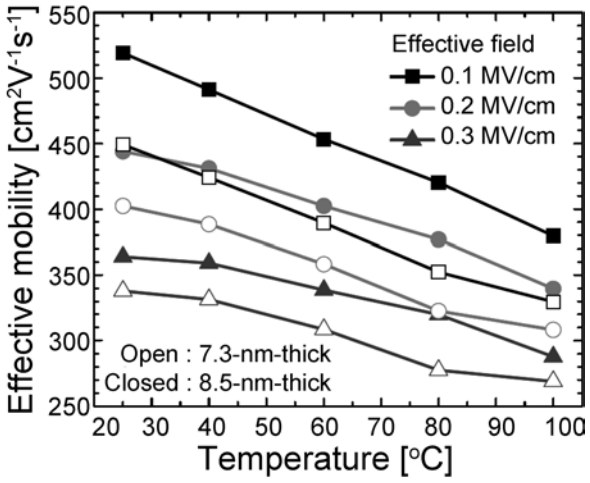

Fig. 8. Effective mobility as a function of operating temperature.

higher than that in the 4.5-nm one. This was attributed to the following two facts. The first is related to the top silicon layer thickness. In general, it should be noted that the top silicon layer thickness determines the area of the depletion region located between the body and drain. Thus, more electrons can be generated in the region of a p-type body to an n^+-type drain junction at 0.1 V drain bias because the area of the depletion layer of a thick UTB SOI n-MOSFET is larger than for a thin ones.

The second is that the leakage current of 8.5-nm-thick UTB SOI n-MOSFETs depends more strongly on temperature than for 4.5-nm-thick ones. The leakage current increment slope of an 8.5-nm-thick UTB SOI n-MOSFET depending on the operation temperature is 2.6 times steeper than for a 4.5-nm-thick one. It is notable that the relationship between the *S* value and the leakage current of UTB SOI n-MOSFETs in the temperature and top silicon layer thickness is in a trade-off relation, as shown in Fig. 5(b) and Fig. 6.

Fig. 7 shows the dependence of the effective mobility of 4.5, 7.3, and 8.5 nm UTB SOI n-MOSFETs. It is known that the effective mobility as a function of the effective field (E_{eff}) is dominated by coulombic scattering in the effective field range of less than 0.05 MV/cm and by phonon scattering in the effective field range from 0.05~0.5 MV/cm [21]. As the effective mobility decreases with an increase in the temperature, the mobility is dominated by a decrease in the phonon scattering, as shown in Fig. 7. The result is that the phonon scattering and increased abruptly by raising the operating temperature of an UTB SOI n-MOSFET and the mobility of all samples decreased with temperature. Although these phenomena occur in all top silicon layer thicknesses UTB SOI n-MOSFETs, a 4.5-nm-thick UTB SOI n-MOSFET's effective mobility is the lowest energy than the others because its channel electrons can be easily affected not only by the scattering due to surface roughness, but also scattering from interfacial roughness. In addition, it was confirmed that the mobility in the electric field regions dominated by coulombic scattering did not vary with an increase in the temperature.

Fig. 8 shows the effective mobilities of 7.3- and 8.5-nm-thick SOI n-MOSFETs as a function of operating temperature. Three lines in Fig. 8 correspond to the

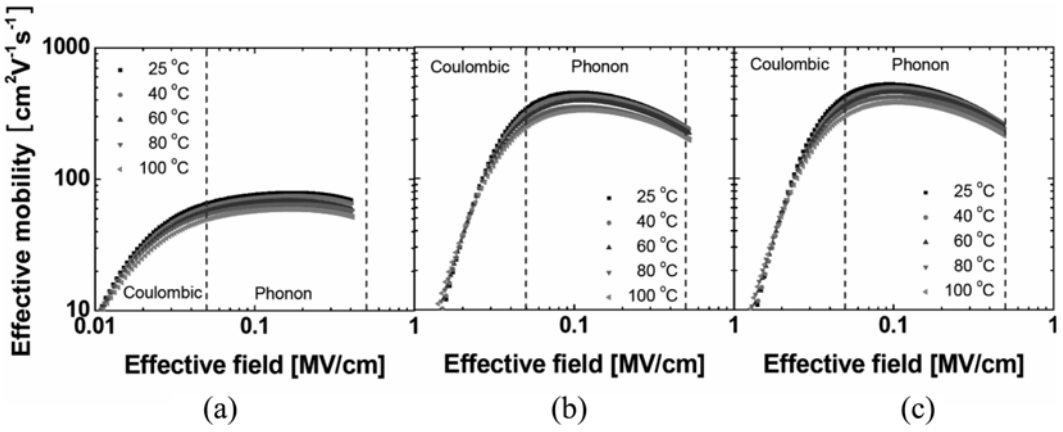

Fig. 7. Effective mobility as a function of effective field as a function of operating temperature, (a) 4.5 nm, (b) 7.3 nm and (c) 8.5 nm-thick top silicon layer UTB SOI n-MOSFETs.

effective mobility extracted at the condition of effective fields of 0.1, 0.2, and 0.3 MV/cm. It was observed that the mobility difference between the effective fields of 0.1 and 0.3 MV/cm decrease with a rises in temperature.

This phenomenon can be explained by the fact of that the effective mobilities in these three regions of the effective field are mainly determined by phonon scattering rather than the scatterings due to surface roughness when the transistor is operated at room temperature. However, if the operating temperature rises, the effective mobilities are likely to be suppressed by the increase in phonon scattering. This was confirmed in Fig. 7(c) which shows that the mobility slope increased positively from -0.338 at 25 °C to −0.266 at 100 °C in an 8.5-nm-thick UTB SOI n-MOSFET [22].

Conclusions

In summary, we successfully fabricated 4.5-, 7.3-, and 8.5-nm-thick UTB SOI n-MOSFETs and investigated the effect of operating temperature on their electrical properties such as subthreshold slope, leakage current, and effective mobility. It was observed that as the temperature rises, the increase in the subthreshold slope was two times greater in the 4.5-nm-thick UTB SOI n-MOSFET than in the 8.5-nm-thick one, and the increase in the leakage current increment ratio in the 4.5-nm-thick was 0.38 times smaller than in the 8.5-nm-thick one. In addition, an increase in the temperature led to a decrease in the effective mobility in the effective field range from 0.05 to 0.5 MV/cm, considered to be the region dominated by as a phonon scattering.

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