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InP/InGaAs/InP DHBT structures with N^+ doped composite collectors grown by gas source molecular beam epitaxy

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InP/InGaAs/InP double heterojunction bipolar transistor (DHBT) structural materials with N^+ doped composite collectors were designed and grown successfully by gas source molecular beam epitaxy (GSMBE). High-quality lattice-matched InGaAs/InP hetero epi-layers were obtained through optimizing the growth conditions. The performance of InP/InGaAs/InP DHBTs with a thin heavily doped n-type InP layer at the base-collector interface was also demonstrated. It was shown that the energy barrier between the base and collector was effectively eliminated by a 3 nm thick n-type InP layer with $N_D=3\times10^{19}$ cm^{-3}. The DHBT devices with an emitter size of 2×12 μm^2 showed $f_T > 80$ GHz and BVceo > 9 V, which can be comparable to the results reported for DHBTs with a graded layer between the base and collector.

Key words: InGaAs/InP, Molecular beam epitaxy (MBE), Energy barrier, Doping, Double heterojunction bipolar transistor (DHBT).

Introduction

InP/InGaAs/InP double heterojunction bipolar transistors (DHBT) are suitable for microwave power and analog circuit applications due to the high breakdown voltage achieved by the lower impact ionization rate of InP, which allows thinner collectors for higher speed without sacrificing the breakdown voltage. The high thermal conductivity of InP is also advantageous for power device applications. While the breakdown voltage of a DHBT benefits from the use of a high band gap collector, the potential barrier at the base-collector (B-C) junction due to the conduction band discontinuity can result in a high saturation voltage in the common-emitter current–voltage (*I–V*) characteristics as well as gain compression. Intensive investigations on various B-C junction designs have been conducted to solve such a problem. InP/InGaAs chirped superlattice (CSL) [1, 2], step-graded InGaAsP [3, 4] and linearly graded InGaAsP [5] junctions have been used on InP collectors. Elimination of the barrier by doping is also an alternative method. It was first proposed by Sugiura et al. who reported on the DC performance of DHBTs with a 30 nm thick n-type InP layer ($N_D=3\times10^{17}$ cm^{-3}) between the InGaAs base and InP collector layers [6]. In this paper, we report on InP/InGaAs/InP DHBT structural materials designed and grown on (100) SI-InP substrates by gas source molecular beam epitaxy (GSMBE). High-quality lattice-matched InGaAs/InP hetero epi-layers were obtained through optimizing the growth conditions. The performance of abrupt InP/InGaAs/InP DHBTs with a thin heavily-doped n-type InP layer at the base-collector interface was also demonstrated. Our main intention to develop N^+ doping composite collector DHBTs originates from the fabrication hurdles related to wet etching of the GaInAsP grade because the wet etch solution for GaInAsP etches InGaAs at a much faster rate so that care must be taken to protect the base layer during wet etching of the grade layer.

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Experiments

The DHBT structural materials were grown by a V90 GSMBE system. Si and Be served as sources for n-type and p-type dopants, respectively. Group-V arsenic and phosphorus beams were obtained by thermal cracking of arsine (AsH_3) and phosphine (PH_3) at a high temperature. 7 N-purity elemental gallium (Ga) and indium (In) were used as the group-III sources. The material structure of an InP-baesd DHBT is shown in Figure 1. A 3 nm thick silicon doped n-type InP layer with $N_D=3\times10^{19}$ cm^{-3} was inserted between the InGaAs base and InP collector layers.

A Philips X'Pert high resolution X-ray diffractometer was used to evaluate the crystalline quality of the epi-layer and its mismatch with substrate. From the rocking curve shown in Fig. 2, it was shown that the full width at half maximum (FWHM) of the $In_{0.53}Ga_{0.47}As$ peak is

Layer Name	Material	Thickness (nm)	Doping (cm^{-3})
Cap	InGaAs	200	Si 2E19
Emitter	InP	50	Si 3E19
Emitter	InP	70	Si 3E17
Spacer	InGaAs	5	undoped
Base	InGaAs	50	Be 4E19
Spacer	InGaAs	5	undoped
n+InP	InP	3	Si 3E19
Collector	InP	300	Si 2E16
Buffer	InGaAs	500	Si 2E19
Substrate	InP	350 μm	Semi-Insulated

Fig. 1. Schematic material structure of the InP/InGaAs/InP DHBT.

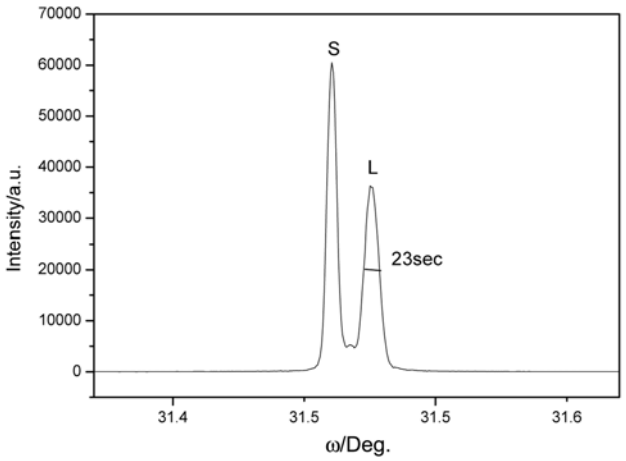

Fig. 2. DCXRD rocking curve of InGaAs/InP hetero epilayer. S, signifies the InP substrate diffraction peak, and L, signifies the InGaAs epi-layer diffraction peak. The analysis results show an indium composition of 52.97%, while the mismatch between the InGaAs epi-layer and InP substrate is 4.25×10^{4}.

Table 1. Electrical characteristics for typical materials used in InGaAs/InP HBT structures

Material	Doping Concentration (cm^{-3})	Mobility (cm^2/V.s)
InGaAs	Si 1.3E19	1757
InGaAs	Be 4E19	51
InP	Si 3E19	650
InP	Si 2.88E17	1710
InP	Si 2.27E16	1913

23 arcseconds, which illustrates good crystalline quality of the hetero epi-layer. The lattice mismatch between $In_{0.53}Ga_{0.47}As$ and InP is as small as 4.25×10^{4}, and the small mismatch signifies a low defect density at the InGaAs/InP hetero-interface. The carrier concentration and mobility of the epi-layers were measured by the Van der Pauw method. Table 1 summarizes the carrier concentrations and mobilities at room temperature of the typical materials used in InP/InGaAs/InP DHBT structures.

The InP/InGaAs/InP devices were fabricated by using photolithography and wet etching. The solutions for etching InP and InGaAs were H_3PO_4:HCl=1:1 and citric acid:H_2O_2=10:1, respectively. The highly selective etching of InP and InGaAs simplifies the fabrication of the device. AuGeNi/Ag/Au and Ti/Pt/Au were adopted as the *n*- and *p*-type Ohmic contact metals, respectively. All the device characteristics of the InP/InGaAs/InP DHBTs were measured using an HP-4155 semiconductor parameter analyzer.

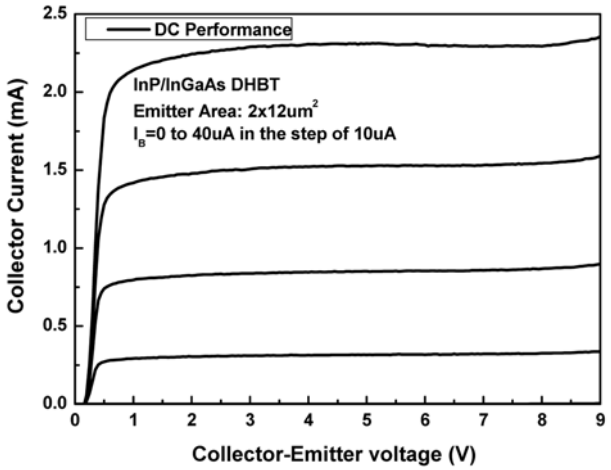

Fig. 3. Common emitter DC characteristics of a 2×12 μm^2 emitter DHBT with a 3-nm-thick doped layer of $N_D=3\times10^{19}$ cm^{-3} at the base-collector interface.

Results and Discussions

The common-emitter DC *I–V* characteristics of the DHBT studied are shown in Fig. 3. Clearly, the barrier was fully eliminated in this structure. As can be seen, it exhibits a low offset voltage of about 50 mV and a DC current gain beyond 70. BVceo is above 9 V. These are possible due to an InGaAs spacer inserted at the BE junction and the lower impact ionization rate of InP used as collector. The common-emitter frequency characteristics of a 2×12 μm^2 emitter device are shown in Fig. 4. The unity current gain cutoff frequency obtained (f_T) is 80 GHz. This indicates this device can satisfy K band circuits application.

To overcome the energy barrier, a calculation reveals

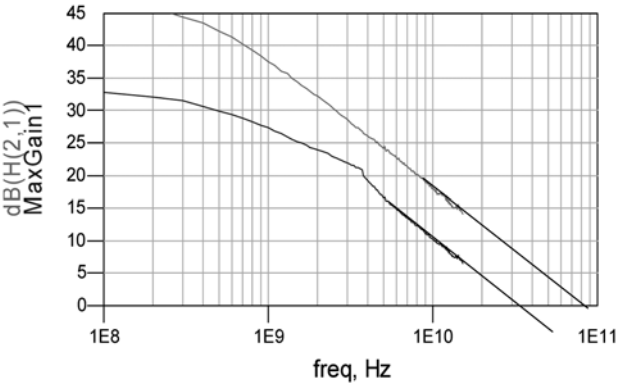

Fig. 4. Common emitter frequency characteristics of a 2×12 μm^2 emitter DHBT with f_T 80 GHz.

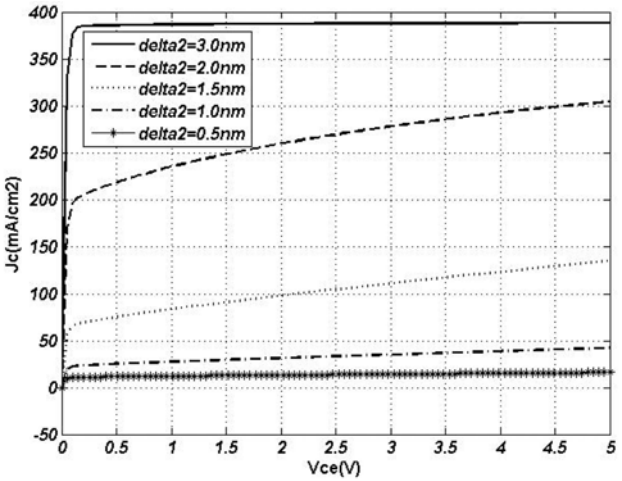

Fig. 5. The dependence of collector current on C-E voltage at different N^+ doping layer thicknesses with a doping concentration of 3×10^{19} cm^{-3}.

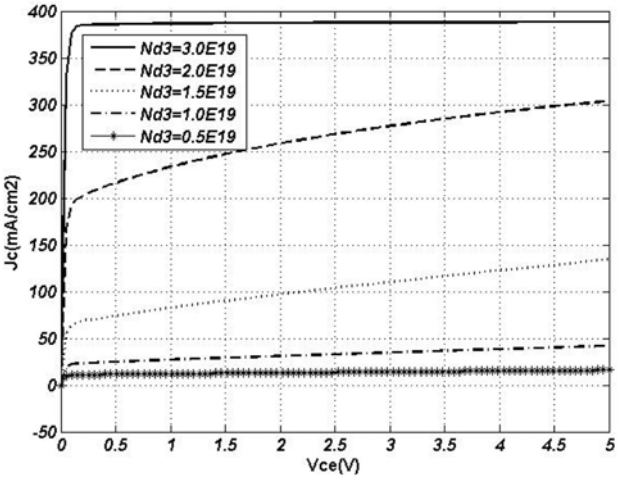

Fig. 6. The dependence of collector current on the C-E voltage at different N^+ doping concentrations with a doping thickness of 3 nm.

the relations between the thickness and doping order of the N^+ Doping layer:

$$\delta_2=\frac{\sqrt{2N_A\varepsilon_2\Delta E_c}}{qN_{D3}} - \sqrt{\frac{2N_A\varepsilon_2\Delta E_c}{q^2N_{D3}^2}-\frac{2N_{D4}\varepsilon_1\Delta E_c+2N_A\varepsilon_2\Delta E_c-2qN_{D4}\varepsilon_1(V_{bi}-V_{BC})}{q^2N_{D3}(N_{D3}-N_{D4})}}$$

where δ_2 is the N^+ doping layer thickness, N_{D3} is the doping concentration and ΔE_c the conduction band offset. Care should be taken not to exceed this thickness because a thicker layer will not be depleted. On the other hand, it will depress the breakdown voltage. Using the Lee and Houston model [7], we calculated the dependence of the collector current on the C-E voltage at different N^+ doping layer thicknesses with a doping concentration of 3×10^{19} cm^{-3}, see Fig. 5 and the dependence of the collector current on the C-E voltage at different N^+ doping layer concentrations with a doping thickness of 3 nm, see Fig. 6. From the calculation, a 3-nm-thick silicon doped InP layer with $N_D=3\times10^{19}$ cm^{-3} is optimal and was used in our InP/InGaAs DHBTs.

Conclusions

InP/InGaAs DHBT structural materials with a 3 nm thick silicon doped InP layer between the InGaAs base and the InP collector layers were designed and grown by GSMBE. The device exhibits a high current gain and low offset voltage due to the existence of the thin heavily-doped n-InP layer, which means that this layer effectively reduces the electron blocking effect at the base-collector interface and improves the performance of InP/InGaAs/InP DHBT devices.

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