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Effect of nano-scale strained Si layer grown on SiGe-on-insulator structure on MOSFET drain current improvement

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Utilizing low-temperature epitaxial technology, we have developed a novel MOSFET structure consisting of a nano-scale (< 15 nm) strained Silicon (Si) layer grown on a nano-scale SiGe-on-insulator (SiGe-OI) structure. By fabricating n-MOSFETs based on this strained Si/SiGe/SiO_2/Si structure, we experimentally studied two effects on the electron mobility in the inversion layer, as compared to MOSFETs based on the conventional silicon on insulator (SOI) structure: the effect of the Ge mole fraction in the SiGe layer, and the effect of the strained Si layer thickness. We observed that the current transport in the strained Si layer was enhanced by a factor of about 1.6 as compared to the unstrained Si in the conventional case. In addition, we found that in the case of a strained Si layer with a thickness of less than 15 nm, as the its thickness was reduced, the electron mobility in the inversion layer decreased.

Key words: nano-thickness, strained- Si, SiGe, mole fraction, phonon scattering rate, mobility.

Introduction

It has been reported that inserting a SiGe layer producing a biaxial tensile strain in the Si inversion layer of an silicon on insulator (SOI) n-Metal Oxide Silicon Field Effect Transistor MOSFET (n-MOSFET) increases the electron mobility [1]. The biaxial tensile strain increases the difference in the sub-energy band between the 2-fold valleys and 4-fold valleys in the conduction band, thus enhancing the occupancy of the 2-fold valleys. As a result, since the effective conduction mass of electrons is smaller in the 2-fold valleys than in the 4-fold valleys, the electron mobility is increased. The effect strongly depends on the Ge mole fraction (x) in the SiGe layer (i.e., a higher Ge mole fraction leads to a higher electron mobility). In addition, as the design rule for SOI MOSFETs drops below 90 nm, the top Si thickness in the SOI is now of the order of tends of nanometers [2]. There have been several theoretical calculations on the dependence of the electron mobility on the nano-scale SOI Si thickness [3]. The electron mobility in the inversion layer of an SOI MOSFET decreases as the Si thickness is reduced in the range of from 20 nm down to 5 nm, yet it increases with reduction in the thickness range from 5 to 3 nm. Gamiz *et al*. [3] showed through simulation that a strained Si inversion layer grown on a SiGe-on-insulator structure would enhance the electron mobility of an SOI MOS-FET as compared to an unstrained Si inversion layer. The electron mobility is thus determined by the thickness of the nano-scale strained Si inversion layer, since the total thickness, including both the strained Si layer and the relaxed SiGe layer, is fixed. That is, the electron mobility decreases with an increasing thickness of a strained Si inversion layer grown on a SiGe-on-insulator substrate [4].

Since this electron mobility improvement has not yet been demonstrated experimentally, in this work, we fabricated n-MOSFETs with a nano-scale strained Si layer grown on a SiGe/SiO_2/Si structure. We then measured the electrical characteristics of the fabricated devices in order to investigate the simultaneous effect of the thickness of the strained Si layer and the Ge mole fraction in the SiGe layer on the electron mobility in the inversion layer.

Device Fabrication and Measurement

Nano-scale Ge epitaxial layers were grown on p-type 200 mm Si wafers with (100) orientation and 10 Ω-cm resistivity by ultra-high-vacuum chemical vapor deposition at 750 °C. The thicknesses of the SiGe layers in our experiment were 3, 5, 8 and 10 nm. A structure consisting of a strained Si layer on a SiGe-OI substrate was fabricated on each wafer by the following process sequence: low-energy hydrogen implantation, room-temperature vertical bonding, low-temperature cleavage (< 400 °C), and high-temperature (> 1125 °C) annealing, followed by chemical etching. The thickness of strained Si was controlled to 5, 7, 10, and 12 nm by varying the chemical etching time. The strained Si layer thicknesses of the experimental samples are summarized in Table 1.

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Table 1. Nano-thickness and Ge mole fraction in the SiGe layer

Sample	T_{Si} (nm)	T_{SiGe} (nm)	Ge Content (%)
No. 1	2.8	10	19
No. 2	5.8	8	14
No. 3	7.8	5	15
No. 4	9.8	3	10
No. 5	12.8	None	0

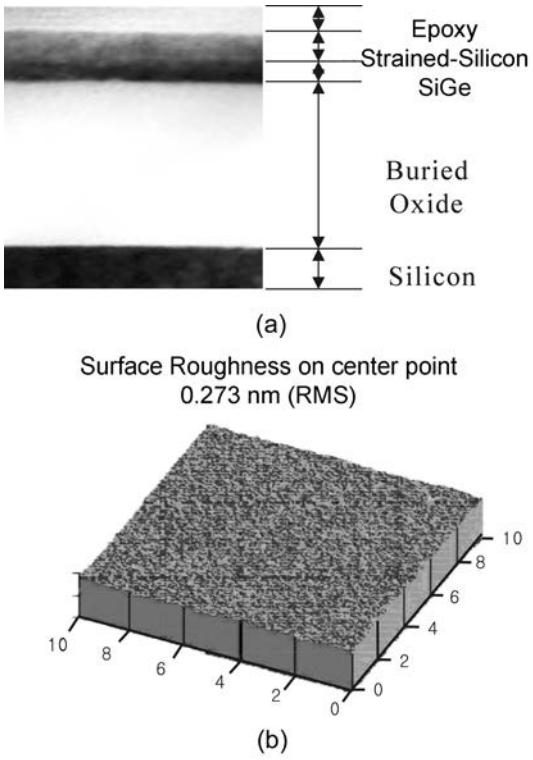

Fig. 1. (a) Cross-sectional TEM image of a strained Si/SiGe/OI structure. (b) AFM image of the rms surface roughness of this structure near the center of a wafer.

A key factor in forming this kind of nano-scale strained Si layer on SiGe-OI is the fabrication of the SiGe-on-insulator (Si/SiGe-OI) substrate layer. Figure 1(a) shows a cross-sectional TEM (transmission electron microscope) image of a nano-scale strained Si layer grown on a $SiGe/SiO_2/Si$ structure. The SiGe layer in Fig. 1(a) appears dark black, in contrast to the silicon layer above. Figure 1(b) shows an AFM (atomic force microscope) image of the surface roughness near the center of the wafer. The rms roughness value is 0.273 nm, indicating almost the same level of surface quality as the bulk silicon.

Figure 2 shows SIMS (secondary ion mass spectroscopy) profiles for all samples as a function of depth. Although the epitaxial process target for the Ge mole fraction in the SiGe layer was 20% for all samples, the final Ge mole fraction in the relaxed- $Si_{1-x}Ge_x$ layer varied from 10% to 20% with the thickness of the layer. This was probably caused by out-diffusion of Ge in the exceedingly thin SiGe layer. The occurrence of a

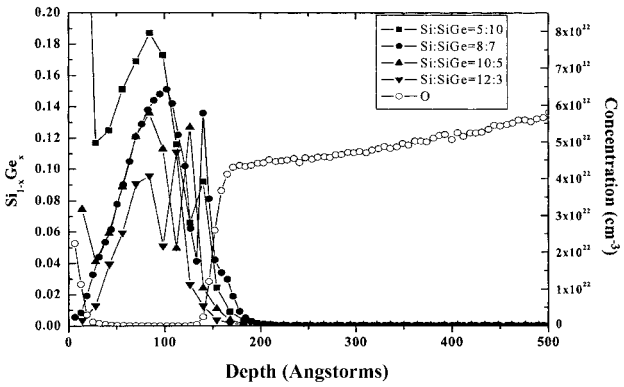

Fig. 2. SIMS profiles of the Ge mole fraction in the SiGe layer for all samples.

second peak of the Ge mole fraction for all samples is attributed to the matrix effect, i.e., when the sputtering O^+ ions used in SIMS contact the buried oxide layer below the SiGe layer, the intensity of secondary electrons is increased.

Since we should exclude the short-channel effect from the current transport characteristics in order to characterize their dependence on both the thickness of the strained Si layer and the Ge mole fraction in the

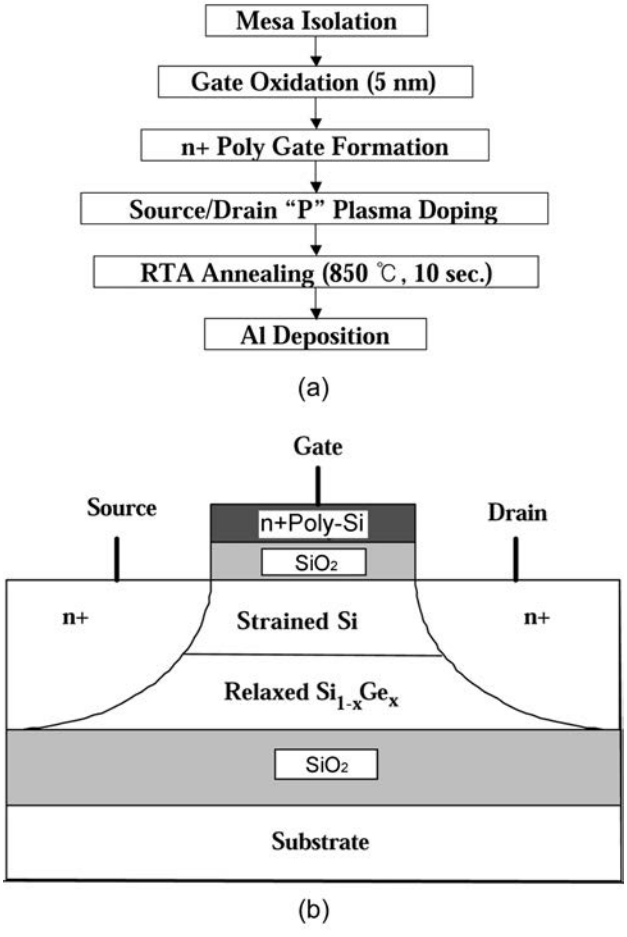

Fig. 3. (a) n-MOSFET device fabrication steps. (b) Schematic structure of the n-MOSFETs.

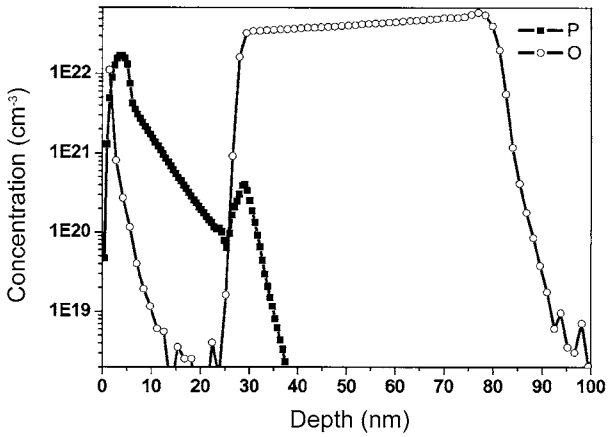

Fig. 4. SIMS profiles of the surface doping concentrations in the source/drain area of an n-MOSFET fabricated by plasma-immersion doping implantation followed by RTA annealing for 10 seconds at 850 °C, The black squares correspond to phosphorous ions, and the open circles correspond to oxygen ions.

SiGe layer at the same time, we fabricated self-aligned, long-channel n-MOSFETs with a form factor ($W \times L$ = 5×5 μm). The process sequence used for fabricating these n-MOSFETs is illustrated in Figure 3(a). The mesa process was utilized to isolate the transistors, and thermal oxidation in a dry O_2 ambient was used to grow a 5 nm thin gate oxide. We confirmed from a C-V plot that the actual gate oxide thickness was 4.88 nm. We then fabricated n^+-doped poly-Si gates, and applied plasma-immersion doping with phosphorous to form the source/drain region, followed by an RTA (rapid thermal annealing) process for 10 seconds at 850 °C to provide activation annealing. Figure 3(b) shows the schematic structure of the long channel n-MOSFETs. Since no channel doping was done, the surface doping concentrations on the source and drain areas were about 2×10^{21} cm^{-3} for all samples, as seen from the SIMS profile shown in Figure 4. For comparison, a conventional SOI wafer without a SiGe layer was processed along with the strained Si samples.

Results and Discussion

Figure 5(a) shows the n-channel drain current vs. drain voltage characteristics of n-MOSFETs fabricated with a strained Si/SiGe/OI structure (solid circles) and a conventional unstrained SOI structure (open circles). The results show that the drain current was enhanced by about 160% in the strained Si/SiGe/OI case as compared to the unstrained SOI n-MOSFET. This enhancement of the current drivability must be attributed to the strain effect. This refers to the well-known fact that a biaxial strain splits a 6-degenerate band into 2- and 4-degenerate bands, resulting in a lowered conduction effective mass and a reduced inter-valley scattering rate [5, 6].

Figure 5(b) show the current characteristics as a

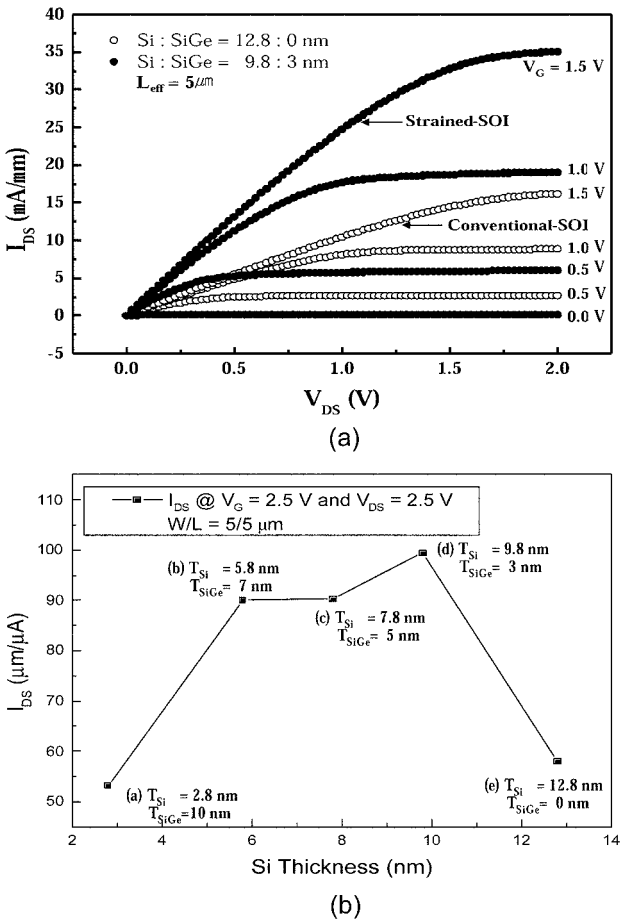

Fig. 5. (a) Experimental drain current characteristics of an n-MOSFET with a strained Si/SiGe-OI structure (Tw = 12.8 nm, T_{Si} = 9.8 nm, T_{SiGe} = 3 nm) compared with those of a conventional SOI n-MOSFET (Tw = 12.8 nm). (b) Drain current characteristics for n-MOSFETs with various thicknesses of strained Si.

function of the strained top silicon thickness. The drain current was measured with a gate voltage of 2.5 V and a drain-to-source voltage of 2.5 V. Except for the device with a 2.8 nm strained Si layer, all the strained SOI n-MOSFETs exhibited a drain current higher than that of a conventional SOI device. The 2.8 nm n-MOSFET likely showed a lower drain current due to a process effect. These results experimentally confirmed, for the first time, that a MOSFET fabricated with a nano-scale ($T_{Si} < 15$ nm) strained Si layer grown on a SiGe/OI substrate can provide a higher current than a conventional SOI MOSFET.

Figure 6(a) shows the conduction effective mass for various values of strained Si thickness and Ge mole fraction. The conduction effective mass was lower for the strained SOI samples than for the unstrained samples. This strongly depends on band splitting, which is a function of the Ge mole fraction. Higher band splitting, due to a higher mole fraction, leads to a higher electron population in the lower band, resulting in a lower conduction effective mass. To distinguish the effect of the thickness from that of the mole fraction, we

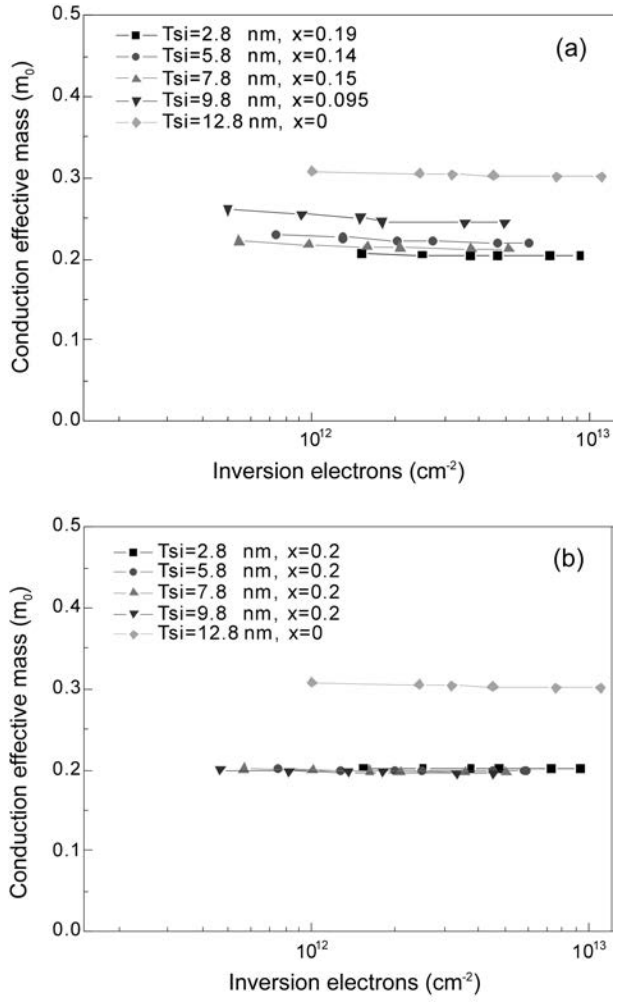

Fig. 6. Conduction effective mass of electrons in strained Si/SiGe-OI inversion layers for various thicknesses of strained Si, with the Ge mole fraction (a) ranging from 0.095 to 0.19 and (b) fixed at 0.2.

calculated the electron mass under the condition of a constant mole fraction. Based on this calculation, Fig. 6(b) illustrates that the effect of the strained Si thickness on the conduction mass is almost negligible. Thus, we have observed that, when the thickness of the strained Si layer is decreased to less than 10 nm and the Ge mole fraction in the SiGe layer is decreased simultaneously, the enhancement of the drain current in a nano-scale strained Si/SiGe-OI MOSFET is subject to two different effects (i.e., the effect of the Ge mole fraction, and the effect of strained Si thickness). In other words, the biaxial tensile strain generated by the Ge mole fraction enhances the drain current, while the decrease in the strained top Si thickness brings about a decrease in the drain currents, as observed in Fig. 5(b).

Conclusion

For CMOSFETs with a 50 nm design rule, we have developed a novel MOSFET structure consisting of a nano-scale of strained Si layer grown on a nano-scale of relaxed SiGe-OI substrate. These novel MOSFETs were fabricated by ultra-high-vacuum chemical vapor deposition at a low temperature. The strained Si layer was found to have not only good crystal quality, without misfit dislocations, but also excellent surface quality, with surface roughness applicable to the sub-50-nm device generation. We observed that the strained Si/SiGe-OI MOSFETs exhibited higher drain current transport than did conventional SOI MOSFETs. In addition, we observed that two effects simultaneously influenced the device performance in terms of the drain current, in that the electron mobility was governed by both the strain effect of the Ge mole fraction in the SiGe layer and the thickness effect of the strained Si layer at the same time. From our experimental results on the strained Si thickness dependency, we found that the drain current was reduced as the strained Si thickness was decreased.

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