JOURNALOF

Ceramic Processing Research

Electrical characteristics of zinc oxide thin film transistor fabricated at high temperature by RF magnetron sputtering technique

M. Amuthasurabi^a, J. Chandradass^{b,*}, V Ramesh Babu^c, P.Baskara Sethupathi^b and M. Leenus Jesu Martin^b

^aPh.D Scholar, Center for Nanotechnology, PRIST, Thanjavur, Tamilnadu, India

^bCentre for Automotive Materials, Department of Automobile Engineering, School of Mechanical Engineering, SRM Institute of Science and Technology, Kattankulathur, Kancheepuram 603203, Tamilnadu, India

^cDepartment of Materials Science and Engineering, National Institute of Technology, Trichy, Tamilnadu, India

We report on the performance of the thin film transistors (TFTs) using ZnO as an active channel layer grown by using radio frequency (rf) magnetron sputtering technique. The TFT device structure used in this study was a bottom gate type, which consists of SiNx as a gate insulator and indium tin oxide (ITO) as a gate deposited onto corning glass substrates. Electrical characteristics of the device showed clear saturation region without any output current degradation due to self heating effect. These ZnO TFTs had a saturation field effect mobility of about 2.14 cm²/Vs, an on to off ratio of greater than 10⁵, the off current of less than 10^{-10} A and a threshold voltage of 15 V at a maximum device processing temperature of 350 °C. This TFT had a channel width of 300 μ m and channel length of 30 μ m. Moreover, the SiNx dielectric layer was found to be optimum for the high performance ZnO based TFTs because of the very low leakage current and good interface between the channel layer and gate material.

Key words: ZnO, Transistor, Self heating Effect, Sputtering, Characteristics.

Introduction

Zinc oxide (ZnO) and doped ZnO, a well-known wide-band gap semiconductor, has drawn much interest because of its transparency and its high channel field effect mobility [1-3]. The ZnO-based TFTs have been intensively studied due to their larger deposition area, non-toxicity and high transparency as well as their compatibility with glass and plastic substrates [4-6]. These properties are applicable and useful for next generation high-resolution electronic display devices and overcome short-comings of conventional a-Si TFTs [7]. But degradation of output current due to heating effect in oxide semiconductor was an important problem which alters the entire characteristics of devices. There were reports analyzed degradation behavior systematically due to presence of self heating effect in silicon based TFTs and in high speed MOSFET [8-9]. In case of zinc oxide few reports were found. Previously we reported the presence of self heating effect gets worsen as the substrate temperature decreases [10]. Therefore substrate temperature is an important parameter to improve the film quality and the device performance. The use of the growth temperature has significant effects on the dopants, defects, and stress in the ZnO films, thus changing their carrier concentration, crystalline structure, optical transmittance, and band gap energy [11-14]. Many research works were analyzed the occurrence of self heating effect in transistor due to low thermal conductivity of substrate and semiconductor layer itself [15-16] and works were done on reduction of this effect as well by improving thermal conductivity of substrate and active layer materials [17-18]. However systematic study was not yet cleared and more study were needed. Many works were proved that the crystallinity of polycrystalline ZnO was improved at higher growth temperature [19-20]. Also alternative gate dielectrics have also been studied to find substitutes for SiO₂ because SiO₂ forms poor interface with ZnO films. Silicon nitride (SiNx) is one of the candidates for ZnO TFTs because it demonstrates better bulk material qualities and forms a better interface with ZnO films. In this article, we report on the fabrication and the characteristics of a bottom-gatetype TFT by using ZnO as an active channel layer and SiNx as a gate insulator layer. The electrical characteristics of thin-film transistors (TFTs) have been investigated to achieve the reduction of self heating effect at higher substrate temperature of 350 °C.

Experimental Procedure

A commercially sintered undoped ZnO target (99.999%) with a diameter of 2 inch was used for the sputtering process. The substrate was a Corning 1737 glass coated

^{*}Corresponding author:

Tel : +91-44-27411905

Fax: +91-44-27452343

E-mail: chandradass.j@ktr.srmuniv.ac.in

with a 190 nm indium tin oxide (ITO) film. Before depositing the insulator layer, substrates were ultrasonically degreased by sequential treatment with trichloroethylene, acetone and methanol for 6 min each and then rinsed with deionized water to remove organic impurities. The gate insulator material was a SiN_x film, deposited using a mixture of SiH₄, NH₃, and N₂ gas by plasma enhanced chemical vapor deposition (PECVD) at a temperature of 300 °C with an rf power of 60 W. The deposition conditions for the gate insulator layer SiN_x to prepare the ZnO TFTs was $SiH_4/NH_3/N_2 = 200/35/800$ sccm at a working pressure of 1 Torr. Then the active layer of the device using ZnO was deposited. Magnetron sputtering was carried out in a mixed atmosphere of oxygen and argon (ratio of 1:3) by supplying an rf power of 80 W. Pre-sputtering was maintained for 10 min in order to clean the target surface. Before starting the deposition, the chamber was evacuated to a base pressure of less than 1×10^{-6} Torr. The sputtering pressure for the ZnO film was maintained at 10 m Torr. The ITO layer was used as the bottom gate contact for the ZnO based TFT device. Undoped ZnO thin films with a thickness of 155 nm were grown by an rf magnetron sputtering technique at a substrate temperature 350 °C. After deposition of the ZnO thin film, source and drain electrodes were patterned using standard photolithography, Ti (30 nm) and Au (90 nm) metal layers were then deposited at room temperature by e-beam evaporation and patterned by means of a lift-off process.

The surface morphology of semiconductor film, schematic device structure of ZnO TFTs and thickness of ZnO channel layer, SiNx gate insulator layer and ITO gate layer were measured by field effect scanning electron microscope (SEM). High resolution x-ray diffraction (XRD) with a Cu K α radiation (1.540 Å) measurement was performed to analyze the crystal quality of the channel layer.The capacitance-voltage (C-V) characteristic of the gate material Ti-Au/SiNx/ITO/Glass structure was measured at 1 MHz and the dielectric constant of the SiNx was determined. The current-voltage (I-V) characteristics and transfer characteristics were measured by means of a semiconductor parameter analyzer (HP 4155A).

Results and Discussion

Fig. 1 shows the surface morphology of semiconductor film grown at 350 °C. The hexagonal shaped crystallites with high densely packed grains with tiny pores resulted. Generally ZnO molecules cannot move easily at low substrate temperatures. So the ZnO films grow in a layer by layer growth mode of two-dimensional 2D first and then in an island growth mode of threedimensional 3D, thus the growth mode would be Stranski-Krasranov mode, resulting in a low crystal quality and a rough surface [21]. But at high substrate temperatures, ZnO molecules can move easily. Hence



Fig. 1. Surface morphology of ZnO film.



Fig. 2. XRD analysis of ZnO film.



Fig. 3. SEM image of cross section view of the device.

the ZnO films exhibit a very smooth surface and a high crystal quality. Also at rf of 80 W enhanced crystallinity obtained because the kinetic energy of the sputtered ZnO molecules is sufficiently high for the molecules to move to the substrate surface in a 3D growth mode. Fig. 2 shows the XRD pattern of ZnO film. The ZnO has a wurtzite structure which shows a strong 001 preferred orientation, perpendicular to the substrate, related to a minimum of the surface energy. Also low structural defects obtained in the diffraction curve. Fig. 3 shows SEM image of device layers. The thickness of ITO, SINx and ZnO layers were 190 nm, 190 nm and 155 nm respectively. Fig. 4 shows the typical drain current (I_D) versus drain-source voltage (V_{DS}) relations at various gate voltages (V_G) for a ZnO TFT. It was observed that the ZnO TFT has an n-channel transistor behavior, since electrons were generated by the positive $V_{G}\ I_{D}$ increases linearly with V_{DS} at low V_{G} and



Fig. 4. Output characteristics of a TFT.



Fig. 5. Input characteristics of a TFT.

saturates at higher V_{DS}. Upon application of positive V_G, I_D increases as the majority carrier (electron) density increases in the channel layer. A high saturation current was about 20 nA under a gate bias of 9 V. The self heating effect along the channel path was not pronounced since perfect saturation obtained in the characteristics. Thus we believe that due to improved crystallinity of the ZnO film grown at higher substrate temperature of 350 °C and reduced structural defects because of optimized sputtering parameters, the distribution of rise in temperature along the channel path at high electric field was uniform which in turn reduce the self heating effect. Also low resistivity with quality ohmic contact of the electrodes was evidenced as crowding effect was minimal at low I_D voltages. Fig. 5 shows the transfer characteristics of the ZnO TFTs with drain voltage of 10 V. ZnO TFT device with a low off current of the order of 10^{-10} A, and an on to off drain current ratio of 10⁵ were achieved. This device shows hard saturation and a positive threshold voltage $(V_{TH} = 15 \text{ V})$, demonstrating that the ZnO TFT operates in the enhancement mode (normally-off characteristics) because the drain current is zero at zero gate bias and a positive gate bias is required for the onset of conduction. From the intercept and the slope of a linear fit to the I_D versus V_{GS} , the saturation field effect mobility (μ_{FE}) and the threshold voltage (V_{TH}) were calculated according to the expression:

$$I_D = \frac{W}{L} C_{SiNx} \mu_{FE} (V_{GS} - V_{th}) V_{DS}$$
⁽¹⁾

where W and L are width and length of the channel, μ_{FE} is the field effect mobility, C_{SiNx} is the capacitance per unit area, V_{GS} is the gate-source voltage and V_{TH} is the threshold voltage. The C-V measurements of ZnO TFTs were performed using the relation,

$$C_{SiNx} = \varepsilon_{oSiNx} A / T_{SiNx}$$
⁽²⁾

(where ε_o is the permittivity of free space, A is the cross sectional area of SiNx, and T_{SiNx} is the thickness of SiNx), the gate insulator capacitance (C_{SiNx}) was calculated to be 1.6×10^{-11} F/m².

The transfer characteristics of the ZnO TFT such as the saturation field effect mobility as high as 2.14 cm^2 /Vs and the threshold voltage of 15 V were achieved. Additionally, the TFT device parameter is mostly related to the crystallinity of channel layer, lower impurities (low oxygen vacancies and/or Zn interstitials), quality of the gate insulator material and channel layer dimensions. It is very important to optimize these parameters effectively in order to obtain the good performance of the device characteristics.

Conclusions

We have fabricated the ZnO based TFTs on corning glass by rf magnetron sputtering. The electrical characteristics showed the absence of self heating effect due to good crystalinity of ZnO semiconductor film grown at high temperature and optimized sputtering parameters. Also the use of silicon nitride dielectric layer improves the interface quality and enhances the device performance by reducing the leakage current. The result shows very good electrical characteristics with a field effect mobility of about 2.14 cm²/Vs, an on to off ratio greater than 10^5 , the off current of less than 10^{-10} A and a threshold voltage of 15 V.

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