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Influence of temperature on self-heating effect in ZnO based thin film transistor fabricated by magnetron sputtering technique

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Zinc oxide (ZnO) channel layer transistors in inverted staggered type were fabricated by magnetron sputtering at different temperatures. The deposition condition of ZnO thin films were analyzed by a field-emission scanning electron microscope and X-ray diffraction measurement and the surface morphology of films were improved by the optimized sputtering parameters. The electrical characteristics of device showed the presence of self-heating effect. The self-heating effect was more pronounced by lowering the temperature due to the creation of more defects in the channel material. It act as traps for charge carrier and degrade the drain current of device which in turn alters the overall device parameters. Current-Voltage characteristics were measured and relevant transistor parameters were calculated and tabulated. The self-heating effect at different temperatures was compared.

Key words: ZnO, Transistor, Sputtering, Film, Temperature.

Introduction

Pure and impure zinc oxide (ZnO) channel materials in thin film transistors (TFTs) are extensively employed in many devices such as flat panel display, organic light emitting displays, fully transparent displays, liquid crystal displays and sensors [1-4]. The cheaper substrate of glass or polymer is necessarily used for lowering the production cost. Therefore various process of depositing doped and un-doped polycrystalline Zinc oxide at low temperature has been utilized to achieve better crystallization [5-8]. The more advantageous technique of depositing ZnO thin films was sputtering where better adhesion and higher density were procured at low and even room temperatures as compared to other methods [9, 10].

Previously many authors have exhibited reasonably high field effect mobility in a TFT using ZnO having device structure, dimensions and even low process temperature [11-14]. Even though the ZnO based TFTs performance were more satisfied for practical application, the material chemistry and device physics need more study to overcome drawbacks of imperfect channel saturation dealt with low temperature. Many authors reported the occurrence of imperfect channel saturation at low temperature polycrystalline silicon based TFTs and scaled down MOSFET devices was due to the presence of self heating effect [15, 16]. But in the case of ZnO based TFTs there are few reports on this effect. Recently, the presence of self-heating effect (SHE) in ZnO based TFT grown at 100 ºC is reported [17]. Here, we investigate the effect of self-heating by varying the deposition temperature (50 ºC and 150 ºC) of the channel material that affects the electrical and structural properties of the devices. The obtained results were compared and tabulated. Moreover, the processing technology would be compatible with inexpensive plastic or flexible substrate.

Experimental Procedure

Thin film transistor was fabricated using the same procedure as reported elsewhere [17]. The glass substrates coated with ITO were taken. A sintered undoped 2-inch-diameter of commercially available 99.999% pure ZnO target was used for radio frequency (RF) magnetron sputtering. ZnO films at 50 ºC and 150°C were deposited over SiNx dielectric layer. The working pressure was maintained at 10 mtorr and RF power was 80 W. For compensating the oxygen vacancies of the zinc oxide crystal, oxygen gas was used along with argon gas. Thus the $Ar:O_2$ gas mixture in the ratio of 3 : 1 was used during film deposition. The low deposition rate of around 4nm/min with the distance of 10 cm between the target and the substrate were maintained in order to allow more time for newly arrived species to combine in low energy configuration to achieve better uniformity while depositing films. These optimized sputtering parameters were kept same for different temperatures of zinc oxide films.

The substrate was indium-tin-oxide (ITO) film coated

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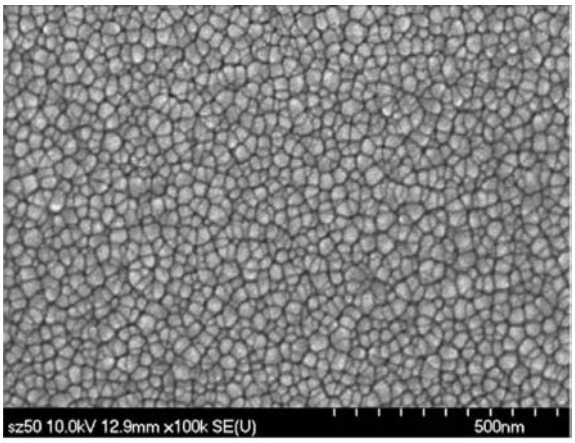
glass with a film thickness of 190-nm. The ITO layer was used as a gate layer for TFT devices. The organic impurities on the substrates were removed ultrasonically with trichloroethylene, acetone, and methanol for 5 minutes in each solution, and rinsed in de-ionized water. By plasma enhanced chemical vapor deposition (PECVD) method the insulator layer of SiNx film was deposited. Using RF magnetron sputtering technique low temperature ZnO thin films at 50 ºC and 150 ºC were grown with the conditions as described above. In order to clean the ZnO target surface the pre-sputtering was maintained for 10 minutes. After the low temperature ZnO films had been deposited, the substrates were patterned using photolithography. The source and drain electrodes were formed using Ti/Au metal deposition and lift off process. The zinc oxide grown at 50 ºC and 150 ºC based TFT devices were subjected to annealing treatment at low temperature of 100 ºC for 15 minutes.

Field-emission scanning electron microscope (FE-SEM) was used to study the surface morphology of ZnO films grown at 50 ºC and 150 ºC. The film thickness of various layer were also measured by FE-SEM. The crystal quality of the channel layer was analyzed by high resolution x-ray diffraction (XRD). Semiconductor parameter analyzer (HP 4155 A) was used to study the output characteristics (I_D-V_{DS}) under various gate voltages (V_{GS}) and the I_D-V_{GS} transfer characteristics under a V_{DS} of 10 V for the fabricated devices.

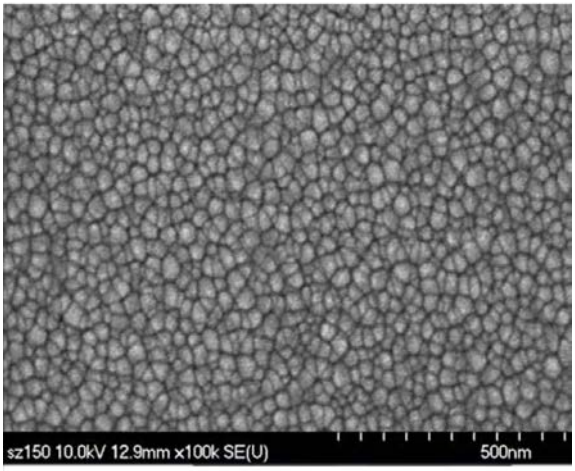
Result and Discussions

Fig. 1 show the SEM image of ZnO films grown at 50 ºC and 150 ºC. At low substrate temperature ZnO molecules cannot move easily, so films grow in a 2-D layer by layer growth mode and then in a 3-D island growth mode results in low quality. But the surface morphology of low temperature ZnO film improved at low deposition rate. The surface morphology did not reveal measurable change in grain size for the semiconductor layer grown at 50 ºC and 150 ºC but there is significant change in occurrence of more grain boundaries in the semiconductor layer grown at 50 ºC. X-ray diffraction measurement (Fig. 2) also shows more defects in the semiconductor layer grown at 50 ºC than 150 ºC. However the smoothness of films was improved by proper control of growth parameters during sputter.

Fig. 3 show the output characteristics of device grown at 50 ºC and 150 ºC taken between the output current (I_D) and output voltage (V_{DS}) at various input gate voltage (V_{GS}) ranging from 0 V to 12 V. These output characteristics showed the occurrence of overshoots and the output current (I_D) begins to decrease at the output voltage (V_{DS}) of 7.5 V and above instead of attaining saturation. The effect is more pronounced in device grown at 50 ºC than 150 ºC. This improper saturation occurs due to self heating effect as the device cannot effectively dissipate the heat evolved in the channel being a poor thermal conductivity of glass substrate. The presence of SHE fabricated at 100 ºC was reported elsewhere [17]. In the present study, the SHE effect was compared with respect to different growth temperatures of device. The creation of more



(a)



(b)

Fig. 1. Surface morphology of ZnO film grown at (a) 50 ºC; (b) 150 ºC.

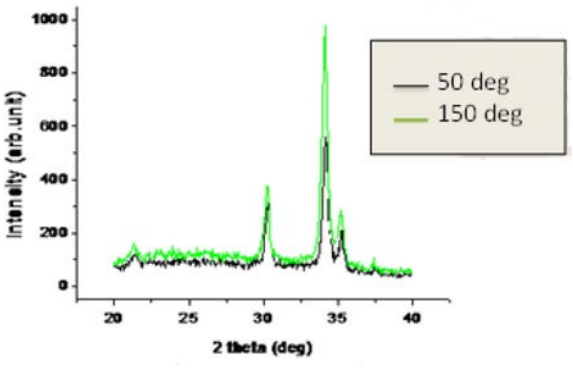


Fig. 2. XRD analysis of ZnO film grown at different temperatures.

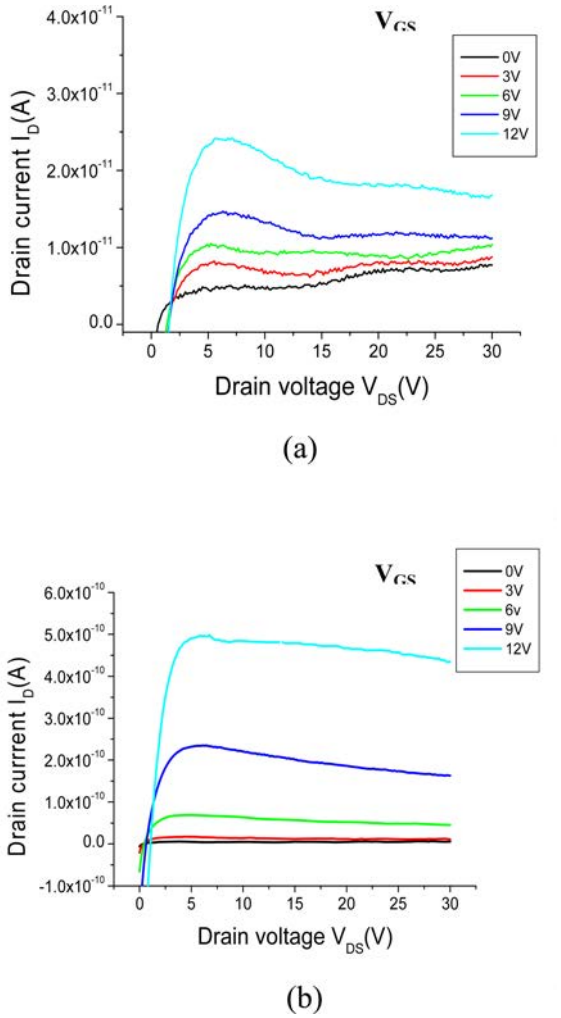


Fig. 3. Output characteristics of a TFT grown at (a) 50 ºC; (b) 150 ºC.

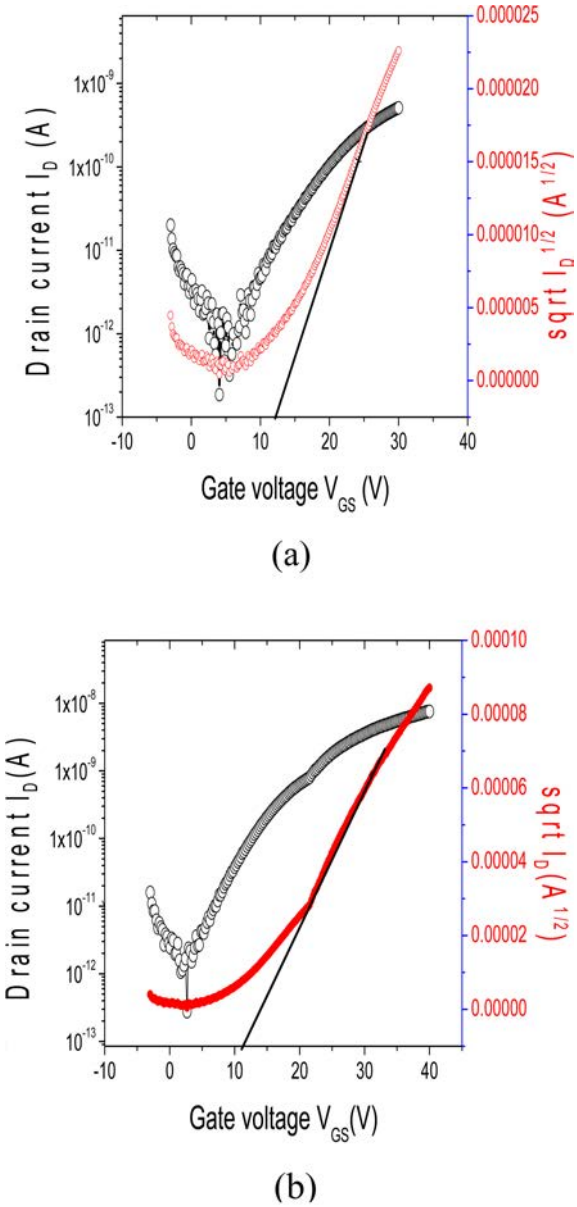


Fig. 4. Input characteristics of a TFT grown at (a) 50 ºC; (b) 150 ºC.

free carrier and grain boundaries in the channel layer induce heating effect as growth temperature of semiconductor layer lowers. These defects can form trap, extend the resistance and rise temperature along the channel path to generate further defects which in turn decreases the charge density and hence the mobility of the channel layer. As a result of increasing the gate and drain voltages in the device, the output current decrease continuously. The effects of self-heating in poly-Si TFTs was very much depend on stress pulse width and thickness of the glass substrate and increase of trap states in the grain boundaries cause temperature rise in device respectively [18, 19]. Liu et al. [11] and Verma et al [2] reported the device with decreased drain current instead of saturation at the output characteristics with no explanations. Fig. 4 show the input characteristics taken between output current (I_D) versus input voltage (V_{GS}) at $V_{DS} = 10$ V) of transistor fabricated at 50 ºC and 150 ºC respectively. A straight line was drawn in the linear region of the square

Table 1. Parameters of TFT.

Temp (degree)	Threshold voltage (V_{TH})	Mobility (μFE) $cm^2/V.s$	Sub threshold slope (S) V/decade	Leakage current (Amp)	On/off ratio
50	13	0.59	6.25	~ 10^{-12}	~ 10^5
150	11	3.39	1	~ 10^{-12}	~ 10^5

root of I_D-V_{GS} to calculate the transistor parameters of field effect mobility μ_{FE}, threshold voltage V_{TH} and sub threshold slope (S) were calculated using the following expressions:

$$I_D = \frac{W}{L} C_{SiNx} \mu_{FE} (V_{GS} - V_{th}) V_{DS} \quad (1)$$

$$S = \frac{dV_{GS}}{d(\log I_D)} \quad (2)$$

Where W is the channel width and L is the channel length. C_{SiNx} is the capacitance per unit area of the insulating layer of SiNx and its value was 1.6×10^{-11} F/ m^2. Also leakage current and on/off ratio were determined. These parameters were tabulated in Table 1. From the table the threshold voltage and sub threshold slope were relatively high at 50 ºC. These values suggested the presence of large density of interface states. A potential barrier with high trap density of the boundary regions was created that will increase threshold voltage and sub threshold swing since it is determined by both the interface states and trap states in the bulk, especially at grain boundaries [20]. Therefore the creation of free carriers and grain boundaries were occurred more in the film grown at 50 ºC than at 150 ºC and in turn create the self heating effect in the transistor.

Conclusions

The output characteristics of ZnO thin films transistor device fabricated at temperature 50 ºC and 150 ºC showed the presence of self heating effect. This effect was increased more as the temperature decreased. It happened because at very low temperature more free carriers and grain boundaries were formed creating potential barrier and defects resulting in temperature along the channel path. Therefore the charge density and the mobility of the channel layer reduced and output current decreased. These defects generate self heating effect which alters the overall performance of the device. Further work is in progress to decrease the SHE to enhance the performance of the device.

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