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Investigation of the structure and electrical properties of strontium titanate thin films growth by pulsed laser deposition method

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In this paper, we have studied the properties of $SrTiO_3$ thin films which have been deposited on Si/Ti/Pt substrates using pulsed laser deposition technique. The as-deposited films were annealed at temperature of 700 °C in oxygen environment for 1 h. The surface morphology, crystalline phase and chemical composition of the films were characterized by AFM, XRD and XPS techniques, respectively. The XRD data show that phase transition from amorphous to polycrystalline structure happens and also the lattice constant enhances during annealing process. This enhancement can be related to oxygen vacancies in thin films. The XPS data show partial lack of titanium atoms on the surface. The AFM analysis indicates that the surface quality of the film is relatively good and the film shows a nanograin structure. Also, the change of leakage current of Si/Ti/Pt/STO/Pt capacitors with applied voltage has been investigated. The results show Schottky barrier for this capacitor.

Key words: $SrTiO_3$ thin films, Pulsed Laser Deposition (PLD), Electrical properties.

Introduction

The insulating dielectric layers used in dynamic random access memory (DRAM) devices should have a large storage density, high dielectric strength and low leakage current, low dielectric loss and longer durability in terms of dielectric breakdown [1-2]. Ferroelectrics and related dielectrics have been suggested for DRAM applications owing to their high dielectric constant, high breakdown strength and low leakage current densities [1]. Strontium titanate ($SrTiO_3$), as a member of perovskite family, with a cubic paraelectric phase [3], is an important dielectric material with an incipient ferroelectric transition (tetragonal-cubic) at 110 K. Above the transition temperature $SrTiO_3$ remains in a single stable cubic phase [4-5]. This material with a dielectric constant of 300, high charge storage density, good insulation and small temperature coefficient of capacitance, has been considered as a possible candidate for an alternative gate insulator in silicon-based metal-insulator-semiconductor (MIS) devices such as DRAMs.

A limiting factor for any DRAM capacitor dielectric is leakage current. In a DRAM cell, the stored charge on the storage capacitor leaks off with time through various leakage mechanisms. This means that the DRAM cells must periodically be taken out of operation so that the stored charge can be refreshed. Thus, the leakage current characteristic of the storage capacitor dielectric is very important in a DRAM cell. The characteristics of electrical conduction were measured using MIM capacitors [6]. A schematic of MIM capacitors has been shown in Fig. 1

In such MIM type capacitors, the metal/insulator interface has a strong influence on the properties, such as the leakage current behavior, cycling stability, and high frequency dielectric losses [7]. A poor interface leads to high leakage currents, higher frequency dispersion and high defect-trapped charges. Therefore, selection of metals for electrodes could strongly effects on the device characteristics. Electrode materials must meet certain requirements such as high conductivity, sufficient resistance against oxidation, good adhesion

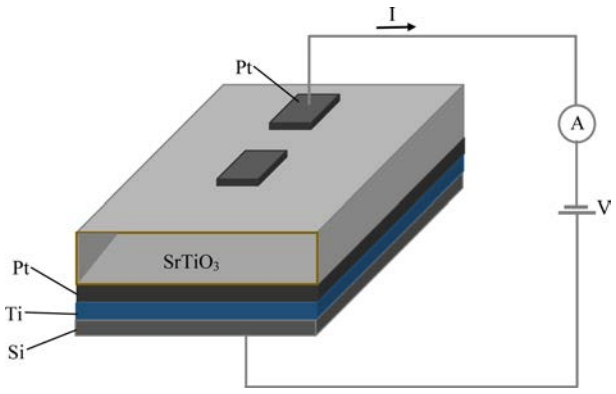

Fig. 1. Schematic diagram of the Si/Ti/Pt/$SrTiO_3$/Pt device.

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to STO and interfacial smoothness to reduce leakage current and increase capacitance. In recent years, metal electrodes such as Pt, Ir and Ru and conducting oxide electrodes such as RuO_2, IrO_2 and $SrRuO_3$ have been investigated for STO varactors. In this study, platinum has been used due to high conductivity and its good oxidation resistance at higher temperatures [8].

In addition, the process of fabrication of the dielectric film should be such that there is minimum interface state density at the insulating film-semiconductor interface [1]. So far various deposition techniques such as sputtering, metalorganic chemical vapour deposition (MOCVD), sol-gel and pulsed laser deposition (PLD) have been used to deposit $SrTiO_3$ films on silicon substrates [9-10]. In recent years, STO films are prepared by PLD method. PLD is a powerful thin film fabrication technique, which utilizes laser beam to evaporate materials and is a successful deposition method to fabricate mixed oxide. The technique of PLD has some advantages over the other techniques, because direct interaction of laser light with the targets reduces film impurity from the environment [1], and the duty cycle of the laser pulses (repetition rate) may easily be varied over three orders of magnitude, providing an insight into the kinetics of the growth process at a fixed temperature [11]. This paper reports results of research obtained from the $SrTiO_3$ thin films in metal-insulator-metal (MIM) structure. The $SrTiO_3$films were grown on a Si/Ti/Pt wafer using the PLD method. The films were characterized using atomic force microscopy (AFM), X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS). In addition, the leakage currents of Si/Ti/Pt/$SrTiO_3$/Pt capacitors have also been investigated.

Experimental

$SrTiO_3$ thin films were grown by pulsed-laser deposition technique on Si/Ti/Pt substrate. The base vacuum pressure was 8×10^5 Torr and the $SrTiO_3$ target was placed at a distance of 4 cm from the substrate. The temperature of substrates was kept at 350 °C during ablation. The PLD process was carried out in a 100 mTorr oxygen (purity 99.999%) environment. We used 5000 pulses of a KrF laser ($\lambda = 248$ nm, energy density 300 mJ/pulse and R.R = 10 HZ) to ablate the STO target. To avoid texturing, the target was rotated at 16 rpm during deposition process. The surface topography, crystalline phase and chemical composition of the thin films were characterized by AFM, XRD and XPS techniques, respectively.

The Platinum bottom electrode with a 200 nm thickness was deposited by electron beam gun technique on the Si//Ti substrate at room temperature. Post annealing of Si/Ti/Pt/$SrTiO_3$ capacitors were performed at 700 °C for 1 h under O_2 atmosphere to introduce oxygen into the STO films surface. Several Platinum dots were evaporated on the films through a mask to form MIM capacitors. The leakage currents of Si/Ti/Pt/$SrTiO_3$/Pt capacitors were measured using a potentio-state analyzer at room temperature.

Results and Discussion

The XRD analysis was used to investigate the effect of annealing on crystalline structures of the STO films. As it is shown in Fig. 2, XRD data of the as-prepared film revealed an amorphous structure. Crystallization of the films strongly depends on annealing temperature. As the annealing temperature increases, the peaks in the XRD pattern become sharper (not shown here). XRD spectra of samples annealed at 700 °C for 1 h in oxygen, show well defined diffraction peaks, and the d values corresponding to XRD peaks were compared with those from JCPDS file 5-634, indicating that the film has been crystallized in $SrTiO_3$ perovskite structure. The lattice constants calculated from the d values of peaks in the X-ray diffraction pattern were [12] a = 0.3917 nm and c = 0.3935 nm according to JCPDSNo.00-003-0769 standard card. Therefore there is an increase in the lattice parameters of the film in comparison to the bulk value (0.3905 nm). This enhancement can be related to the presence of oxygen vacancies, defects in the film structure and the difference in the thermal expansion coefficients of the substrate and that of the $SrTiO_3$ film [13].

X-ray photoelectron spectroscopy (XPS) was used to study the chemical states and abundances of the constituent elements [14]. Figure 3(a,b) shows high resolution spectra of Sr3d and Ti2p peaks for STO films. The binding energy of the $Sr3d_{3/2}$ and $Sr3d_{5/2}$ peaks is centered at 134.6 and 132.8 eV which indicates strontium is present in the form of Sr^{2+} [8].

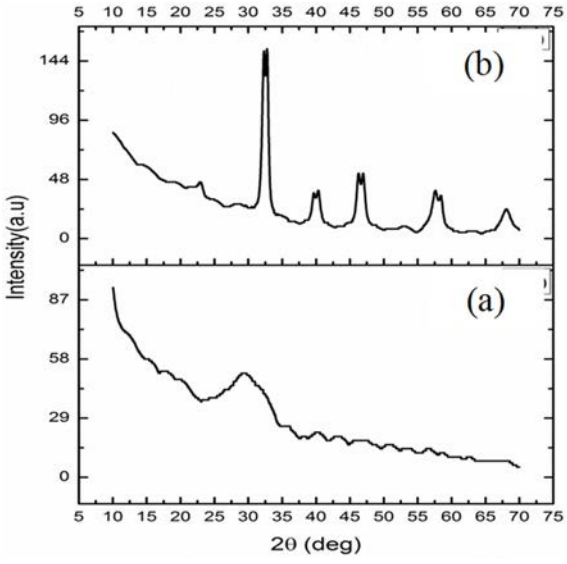

Fig. 2. X-ray diffraction patterns of $SrTiO_3$ thin films (a) as-deposited (b) after annealing at 700 °C.

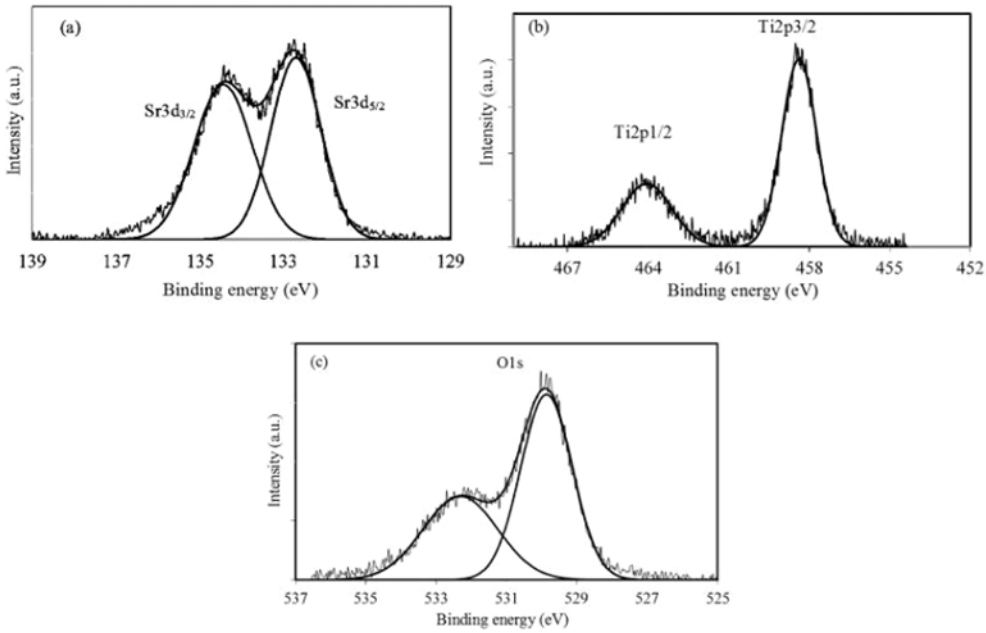

Fig. 3. High resolution XPS spectra of (a) Sr3d and (b) Ti2p peak for $SrTiO_3$ thin film.

Verhoeven and Dorveren have reported same peaks for Sr^{2+} in SrO composition [15]. The high resolution XPS spectra of Ti2p peak is presented in Fig. 2(b). The binding energy of the $Ti2p_{3/2}$ and $Ti2p_{1/2}$ peaks are centered at 458.04 and 463.75 eV, respectively that indicates Ti2p peaks are shifted about 0.9 eV towards lower binding energies in comparison to the Ti2p of the bulk of Ti_2O composition (459.0 eV for $Ti2p_{3/2}$) [4, 9]. Figure 2(c) shows high resolution spectra of O1s XPS peak. The O1s peak is deconvoluted into two components. The main peak at 529.8 eV and the peak observed at 531.6 eV are related to oxygen atoms in perovskite structure STO and oxygen in OH groups or a contamination, respectively.

The ratio of Sr3d/Ti2p, O1s/Sr3d and O1s/Ti2p on the film surface was about ~ 1.4, ~ 2.2 and ~ 3.2, respectively. These ratio indicate additional amount of strontium atoms on the film surface. Therefore the leakage properties of strontium titanate capacitors can be affected. In other word, the reduction of titanium in the strontium titanate structure can lead to the formation of a lot of holes at the dielectric/electrode interface [4]. These holes at the interface layer can lead to the increase of leakage current. In addition, the presence of additional amount of strontium in the STO films affects on the ionic bonding of Ti-O bond results in an enhancement on its length and a decrease in bonding energy [8]. Therefore, as mentioned above, the Ti2p peaks are shifted about 0.9 eV towards lower binding energies.

Major factors limiting the thin film dielectric behaviours are the grain size and surface roughness. The leakage current through the dielectric tends to increase with increasing the grain-size and surface roughness [16]. AFM analysis can be applied as a technique to observe grain size and surface roughness of the STO films. Figure 4 shows AFM image of annealed $SrTiO_3$ film at 700 °C. It can be seen from this figure that the average grain size and average surface roughness (RMS) of the film is ~ 80 nm and 3.27 nm, respectively. Thus the surface quality of the film is relatively good and the film shows a nanograin structure [16]. According to these results, we expect the synthesized STO film can be used as dielectric in MIM capacitors.

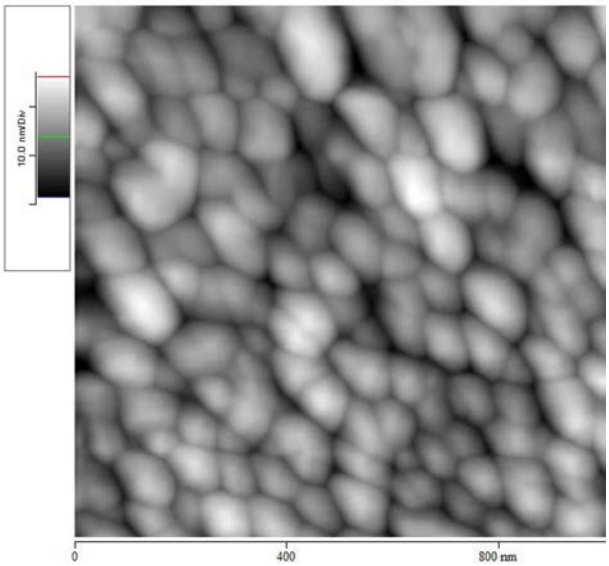

Fig. 4. AFM image of $SrTiO_3$ film after annealing at 700 °C.

Figure 5 shows the change of leakage current of Si/Ti/Pt/$SrTiO_3$/Pt capacitors with applied voltage (I-V curve). The leakage current density curve of the STO films are asymmetric, these imply that the leakage current is electrode-limited. The leakage current in

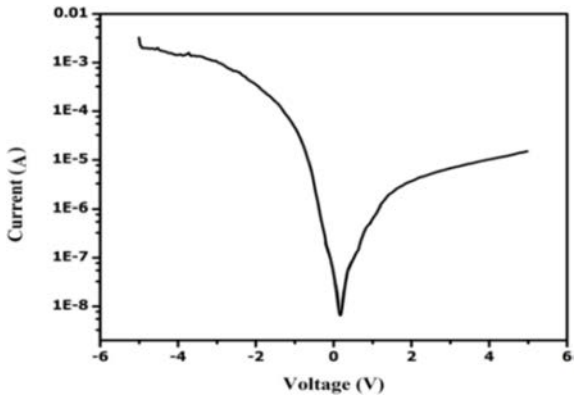

Fig. 5. Change of leakage current of Si/Ti/Pt/SrTiO3/Pt capacitors with applied voltage.

negative bias is mainly affected by the interface between STO and Pt top electrodes [17]. In addition, it can be easily noticed that the reverse current was much higher than the forward current. This behaviour for negative applied voltage is consistent with the fact that the leakage current through STO films has been described as a Schottky-barrier limited current. Hence, when a negative voltage is applied on the platinum electrode, the leakage current is limited by the Schottky barrier [18]. Since positive or negative bias is applied to the top electrode in DRAM operation, such a high reverse current should be reduced as well as forward current to preserve storage charge. The higher reverse current might be caused by a higher generation of oxygen vacancy at the interface with the platinum top electrode. This draw back can be related to diffusion of oxygen from the STO films to the platinum top electrode during Pt electrode deposition. Oxygen vacancy generated by such a process $O_o = V_o^{\cdot\cdot} + 2e^- + \frac{1}{2}O_2$ may act as an electron trap site so it causes a high leakage current of Si/Ti/Pt/$SrTiO_3$/Pt capacitors [15]. To improve the reverse leakage current more work are underway.

Conclusions

In this paper, $SrTiO_3$ films were deposited on Si/Ti/Pt substrate by PLD method. The as-deposited film showed an amorphous nature. The amorphous to polycrystalline phase transition could take place by annealing at 700 °C. XPS analysis shows the reduction of Ti on the film surface. The decreasing of titanium amount in the strontium titanate structure can lead to the formation of a lot of holes at the dielectric/electrode interface and increase of leakage current. AFM image shows the average grain size and average surface roughness (RMS) of the film is ~80 nm and 3.27 nm, respectively. Therefore the surface quality of the film is relatively good and the film shows a nanograin structure. Also, the changes of leakage current of Si/Ti/STO/Pt capacitors with applied voltage indicate that there is a Schottky barrier between STO film and Pt electrode.

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