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Nonvolatile memory characteristics of a multi-stacked MOS capacitor using Ta_2O_5 and $TaAlO_4$ as the charge trap layer

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A flash memory, which uses a floating-gate $SiO_2/Si_3N_4/SiO_2$ (ONO) structure for the next generation, non-volatile memory applications, has serious problems to overcome in the context of scaling down the device size. In this study, $Al_2O_3/Ta_2O_5/Al_2O_3$ (ATA) and $Al_2O_3/TaAlO_4/Al_2O_3$ (A/TAO/A) multilayer films were fabricated to replace the conventional ONO structure. The structures and thicknesses of the multilayers were analyzed by HRTEM and ellipsometry. All films were found to be comprised of amorphous phases, and interfacial layers ($AlSiO_3$) were observed in both films. The electrical properties of the A/TAO/A films were better than those of the ATA films. Program/erase cycle tests were performed, and initial memory windows were maintained after 10^4 program/erase cycles with both films.

Key words: Flash, ONO, Charge trap, High-k dielectrics, Ta_2O_5, $Ta_1Al_1O_4$.

Introduction

Flash memory devices are indispensable components of modern electronic systems such as personal computers, cellular phones, and global positioning systems [1-3]. Over the past decade, many research and development (R&D) programs have focused on improving the capacity, performance, and power consumption of flash memories. However, current flash memory technologies, which use a floating-gate, are difficult to apply below the 25 nm technology node due to cross-talk problems between word-lines and a wide threshold voltage (V_{th}) [4-5]. To solve these problems, devices fabricated with multi-stacked silicon-oxide-nitride-oxide-silicon (SONOS) films instead of a floating-gate have been proposed [6-9]. The lack of floating-gates in SONOS devices prevents a stress-induced leakage current (SILC) and solves the capacitance coupling problem [10-11].

However, SONOS devices also have serious problems including a high erase power and poor retention properties and are difficult to scale down for conventional use [12-13]. In particular, it is impossible to further scale down the tunnel oxide (bottom oxide). According to the 2008 ITRS [14], the tunnel oxide thickness should be about 3-4 nm. It is difficult to achieve this thickness due to the manifestation of film degradation from the leakage current and SILC. The "thickness degradation problem" is similar to the DRAM gate oxide issue ($SiO_2 \rightarrow$ high-k material) that was discovered in early 2000. SiO_2 (tunnel oxide) films less than 3 nm-thick do not function properly due to charge leakage and retention problems, and SILC becomes more serious during device operation when a thin tunnel oxide is used. This causes improper device operation and shortens the device lifetime. Therefore, a SiO_2 layer less than 3 nm cannot be used and should be replaced by other materials that have a higher dielectric constant. Since the physical thickness of a high-k material has an equivalent oxide thickness (EOT) greater than that of ONO, the use of this type of material could potentially solve the thickness degradation problem and improve charge trapping efficiency [15-16]. Ta_2O_5 and Ta-aluminate materials in particular have much lower values of the conduction band offset than other high-k materials. Therefore, the use of these materials as trap layers can be expected to prevent a loss or leakage of the trapped charges due to the wide difference in the conduction band offsets between layers (tunnel oxide-trap layer, blocking oxide-trap layer).

In this study, the memory characteristics of $Al_2O_3/Ta_2O_5/Al_2O_3$ (ATA) and $Al_2O_3/TaAlO_4/Al_2O_3$ (A/TAO/A) multi-stacked films were investigated. Al_2O_3 was used to fabricate the tunnel (bottom) and blocking (top) oxides, and Ta_2O_5 and $TaAlO_4$ (TAO) were used as trap layers.

Experimental Procedures

ATA and A/TAO/A multi-stacked films were deposited onto (100) n-type Si wafers (Siltron, Korea) by a MOCVD (metal organic chemical vapor deposition) system. The wafers were cleaned with organic solvents and were then treated with 10% hydrofluoric acid (HF) solution to remove the native oxide. Al-acetylacetonate [$Al(CH_3COCH)_3$, Strem Chemical. Inc., USA] and tantalum(V) tetraethoxyacetylacetonate [$Ta(OC_2H_5)_4(CH_3COCHCOCH_3)$, Strem Chemical. Inc., USA] were used as precursors for Al and Ta metal, respectively. N_2 gas was used as

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the carrier gas for the Al and Ta metal.

ATA and A/TAO/A films were fabricated by first depositing 5 nm of Al_2O_3 tunnel oxide (bottom oxide) onto the wafer, followed by 5 nm of either a Ta_2O_5 or $Ta_1Al_1O_4$ trap layer on top of the 5 nm Al_2O_3 tunnel oxide. Then, 15 nm of Al_2O_3 blocking oxide (top oxide) was deposited onto the 5 nm trap layer of Ta_2O_5 or $TaAlO_4$.

Film thicknesses were measured with an ellipsometer (Gartner, L117, $\lambda = 632.8$ nm), and the crystallinity of the deposited films was measured by X-ray diffraction (XRD). In order to investigate the formation of an interfacial layer and to confirm the multi-stacked film structure, we performed high-resolution transmission electron microscopy (HRTEM, JEOL 2100F, JEOL). MOS capacitors (Pt/Al_2O_3/Ta_2O_5, $TaAlO_4$/Al_2O_3/Si) were fabricated to measure the electrical properties of the multi-stacked films. The Pt electrode of the capacitor was fabricated using magnetron sputtering with a shadow mask. The thickness of the Pt electrode was approximately 1500 Å, and the capacitor area was 9.25×10^{-4} cm^2. An Agilent B1500A semiconductor device analyzer was used to determine the *C-V* characteristics of the multi-stacked films.

Results and Discussion

Fig. 1 shows the glancing angle XRD patterns of (a) Ta_2O_5 and (b) $Ta_1Al_1O_4$ layers that were deposited for 20 minutes at deposition temperatures ranging from 200 to 450 °C. According to a report by Maeng, *et al*. [17], crystalline Ta_2O_5 in thin films has orthorhombic (α and β phases) and hexagonal (δ phase) phases. The α (above 1360 °C) and β (below 1360 °C) phases occur with a reversible transition at 1360 °C. Additionally, unstable or meta-stable phases, which are either a δ phase or a pseudo-hexagonal phase, appear between 300 and 800 °C. In this study, three peaks that appeared to correspond to a pseudo-hexagonal phase were observed above 250 °C. Unlike Ta_2O_5, $TaAlO_4$ showed a marked resistance to crystallization in that it did not crystallize even after annealing at 450 °C. This observation is consistent with results from previous studies of the crystallization behavior of Al incorporated films (i.e., aluminate) [18]. Since the grain boundaries can affect charge storage and leakage during electrical operations, we chose a deposition temperature of 200 °C, which yielded amorphous phases in both films.

Fig. 2 shows HRTEM images of the (a) Al_2O_3/Ta_2O_5/Al_2O_3 and (b) Al_2O_3/$TaAlO_4$/Al_2O_3 multilayer structures. Since semiconductor injection should be induced during program/erase operations, the blocking oxide was deposited in a layer three times thicker than the thickness of the tunnel oxide [19]. These multi-stacked thin films were deposited at 200 °C, and amorphous phases were observed in both films. Hence, we hypothesized that current leakage through the grain boundaries would be prevented during electrical operation and throughout the retention time of the stored charge.

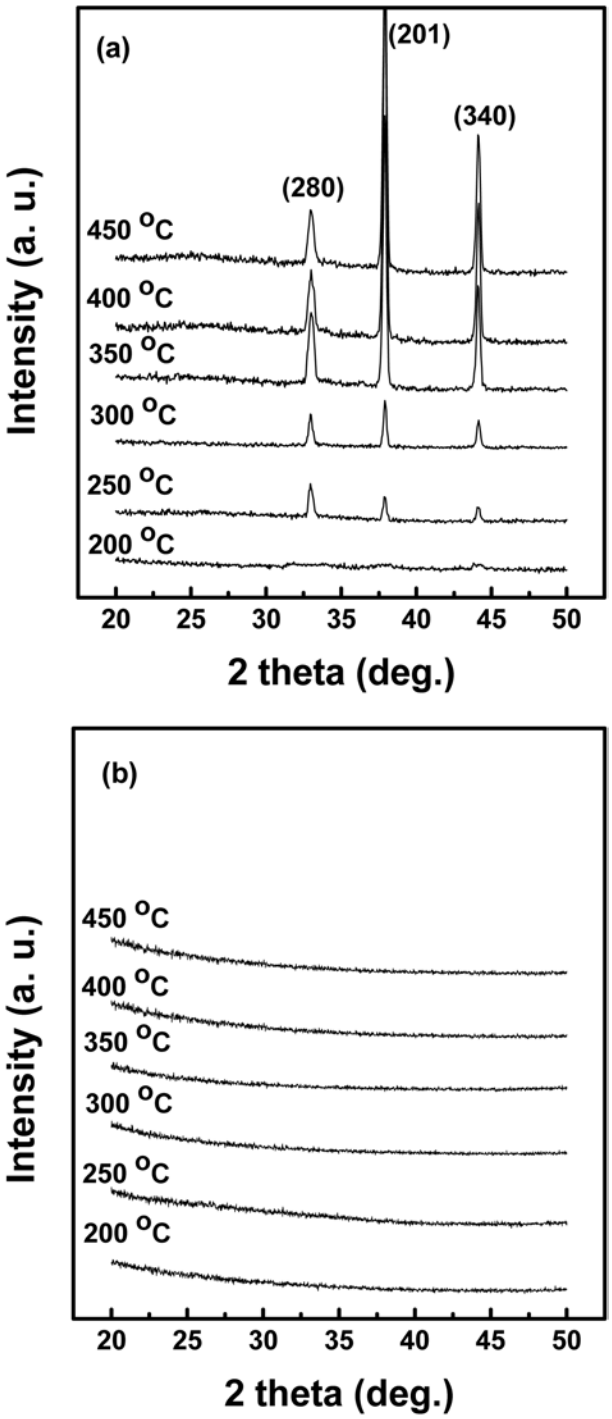

Fig. 1. Glancing angle XRD patterns of the (a) Ta_2O_5 and (b) $TaAlO_4$ films at various deposition temperatures.

An interfacial layer ($Al_xSi_yO_z$) between the Si substrate and the tunnel oxide was observed. Since the conduction band offsets of Al_2O_3 and SiO_2 are 2.8 and 3.5 eV [3], respectively, the mixture of the two results in a higher conduction band offset for the interfacial layer than for a single, uniform Al_2O_3 layer, but a lower conduction band offset than SiO_2. The interfacial layer plays a role in both the electrical operation and the retention of stored charge.

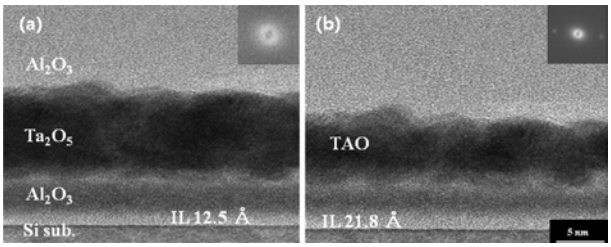

Fig. 2. HRTEM images of the (a) $Al_2O_3/Ta_2O_5/Al_2O_3$ and (b) $Al_2O_3/TaAlO_4/Al_2O_3$ films deposited on Si substrates.

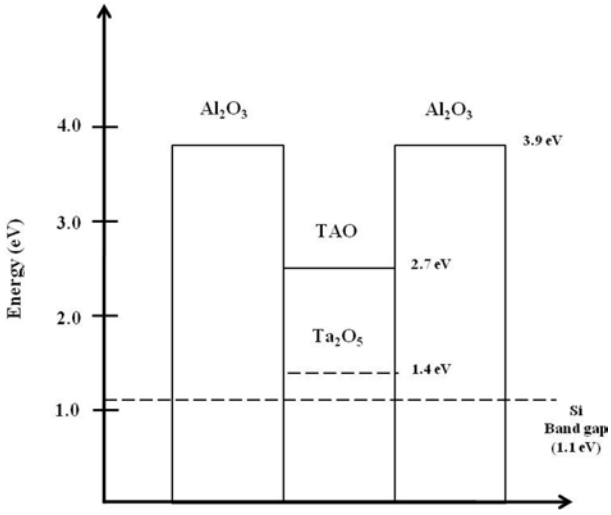

Fig. 2 (c). Energy band diagrams with the conduction band edge of the $Al_2O_3/Ta_2O_5/Al_2O_3$ and $Al_2O_3/TaAlO_4/Al_2O_3$ films.

The film density of the interfacial layer was lower than that of the deposited film since it formed as a result of the chemical reaction between Si and Al_2O_3 during the initial deposition. Because of the low film density and the enhanced stoichiometric characteristics of the interfacial layer, the charge carrier can easily penetrate from the tunnel oxide (interfacial layer + Al_2O_3) to the trap layer during program operation [20]. These conditions can yield more superior program characteristics (i.e., lower operation voltage, shorter program time) than a tunnel oxide without an interfacial layer. Furthermore, the retention characteristics of the stored charge may also improve as a result of the increased interfacial layer conduction band offset [3]. The increased interfacial layer conduction band offset results in an increased barrier height in the tunnel oxide, thereby preventing the stored charge from easily escaping from the film [11].

The interfacial layer also has a shortcoming, however. Since the film density of the interfacial layer is lower than that of a homogeneous, single Al_2O_3 tunnel oxide, failures such as SILC can occur as a result of repetitive program/erase cycles. Hence, the overall effect of the interfacial layer is complex.

Fig. 2(c) shows the energy band diagram with the conduction band edge of the $Al_2O_3/Ta_2O_5/Al_2O_3$ and $Al_2O_3/TaAlO_4/Al_2O_3$ films. The conduction band offset of the charge trap layer should be lower than that of the tunnel and blocking oxides in order to facilitate successful program/erase operations in the charge trap layer. According to a report by Kang [3], the band offsets of Al_2O_3 and Ta_2O_5 on Si were 2.8 eV (3.9 eV-1.1 eV) and 0.3 eV (1.4 eV-1.1 eV), respectively. Although a conduction band offset for $Ta_1Al_1O_4$ on Si has not been reported, it is expected to have a value between 0.3 eV and 2.8 eV as it is a mixture of Ta_2O_5 and Al_2O_3. Therefore, we assumed the value of the conduction band offset of $TaAlO_4$ was the average of the values for Ta_2O_5 and Al_2O_3.

Fig. 3 shows the threshold voltage (V_{th}) shift (full erase (V_{th})-program (V_{th})) of (a) $Al_2O_3/Ta_2O_5/Al_2O_3$ and (b) $Al_2O_3/TaAlO_4/Al_2O_3$ films after a program pulse of 5-13 V over 3-1000 ms. Prior to the program test, a full erase operation was performed at −15 V for 2 s to remove the initial charge carrier in the films. As the program

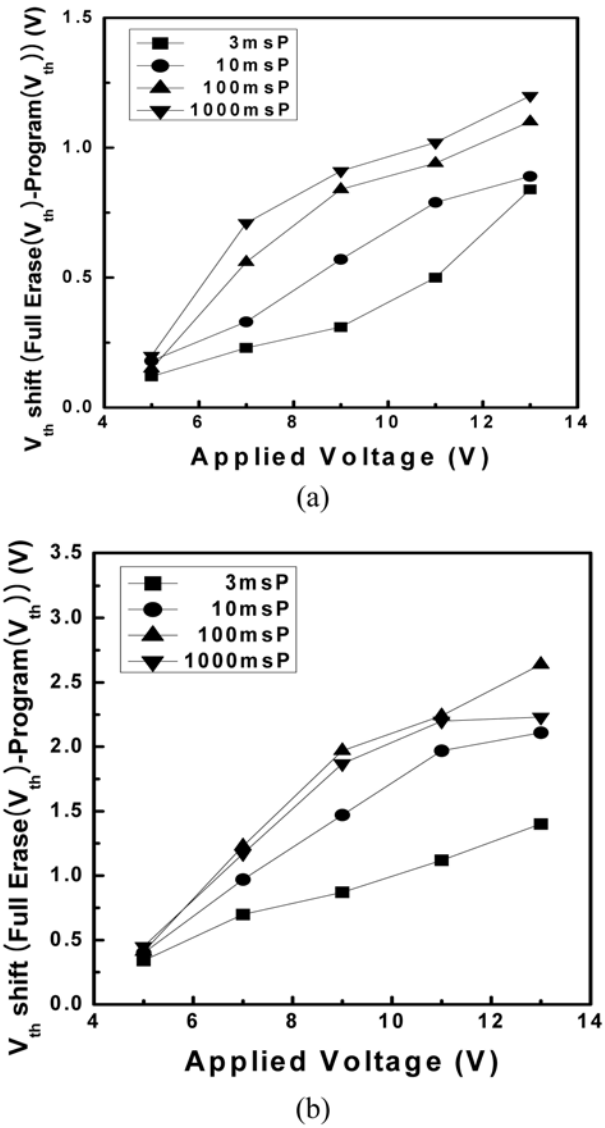

Fig. 3. Threshold voltage (V_{th}) shifts of the (a) $Al_2O_3/Ta_2O_5/Al_2O_3$ and (b) $Al_2O_3/TaAlO_4/Al_2O_3$ films after a program pulse of 5-13 V for 3-1000 ms.

voltage and time were increased, the threshold voltage increased. This indicates that the charge moved from the Si substrate to the trap layer through the tunnel oxide. The charge trapping efficiency of the A/TAO/A films was greater than that of the ATA films. Other researchers [21-22] have reported that Ta_2O_5 does not have a specific defect energy level for charge trapping, and that oxygen vacancies (V_O) and fixed charge (Q_f) both affect the charge trapping properties of Ta_2O_5 films. The carrier moves by the Poole-Frenkel transport mechanism in sites of oxygen vacancies and fixed charge. As a result, the probability of charge trapping is seriously diminished when Ta_2O_5 is used as the trap layer.

Conversely, $Ta_1Al_1O_4$ has an additional trap site (Al_{Ta}^{O}) compared with Ta_2O_5. Although the same defect sites exist in both films [23-24], the defect energy level is higher when Al is incorporated into the films. This indicates that the difference between conduction band offsets [(CB offset of film)-(CB offset of defect), ΔV_{th}] is small. For small conduction band offset differences, charge trapping can occur at a low voltage and for a short time during program operation, and the charge trapping efficiency can increase due to the shallow defect energy level. In this study, the optimized program conditions for the ATA and A/TAO/A films were 11 V for 100 ms and 9 V for 100 ms, respectively.

Fig. 4 shows the fully erased, programmed, and erased *C-V* curves of the (a) $Al_2O_3/Ta_2O_5/Al_2O_3$ and (b) $Al_2O_3/Ta_1Al_1O_4/Al_2O_3$ films. The memory windows [program (V_{th})-erase (V_{th})] of the ATA and A/TAO/A films were 1.225 ΔV_{th} and 2.197 ΔV_{th}, respectively. Since a bi-stable status during the operation of flash memory devices is distinguished by a threshold voltage (V_{th}), the memory window of the device should be wide, at least over 1 V. The memory window of the films with $Ta_xAl_yO_z$ as the trap layer was approximately 80% wider than that of films with Ta_2O_5 as the trap layer.

Two rationales can be proposed for the electrical properties that were observed. First, the interfacial layers of the tunnel oxides differ in thickness. Tunneling of the charge carrier during program operation is affected by the electric field across the tunnel oxide. In the HRTEM images depicted in Figs. 2(a) and 2(b), the total tunnel oxide (Al_2O_3 layer + interfacial layer) thickness was almost the same for both films. However, the interfacial layer was thicker in the A/TAO/A films than in the ATA films. The electric field applied at the interfacial layer in the ATA films was much stronger than at the interfacial layer in the A/TAO/A films as a result of the differing layer thickness, which allows easy tunneling from the substrate to the trap layer. However, the Al_2O_3 layer is relatively dense and is thicker in ATA films. Since the main barrier during program operation is affected by the film density, the tunneling efficiency is expected to be better with A/TAO/A films.

A second explanation is related to the trapping probability in the charge trap layer. In order to trap the charge carrier in the Ta_2O_5 layer, Poole-Frenkel (PF) tunneling must occur.

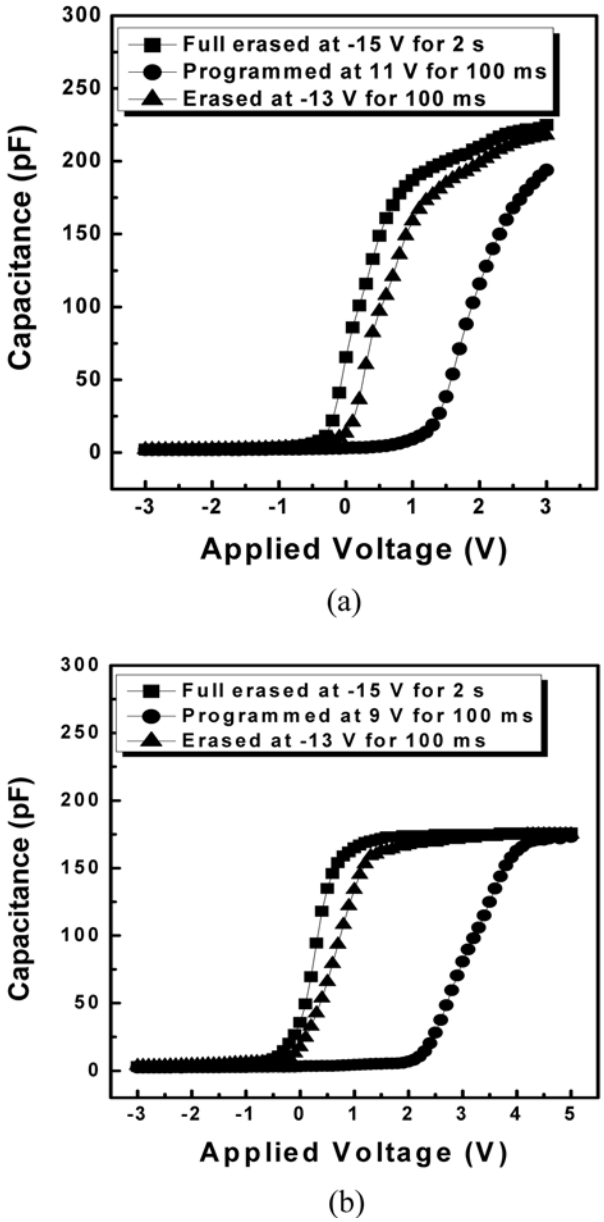

Fig. 4. Fully erased, then programmed and erased *C-V* curves of the (a) $Al_2O_3/Ta_2O_5/Al_2O_3$ and (b) $Al_2O_3/TaAlO_4/Al_2O_3$ films.

However, the fact that additional defects such as Al_{Ta}^{O} exist in A/TAO/A films, make the use of A/TAO/A advantageous compared to ATA films. Therefore, the charge trapping properties of A/TAO/A films are expected to be better than those of ATA films.

Fig. 5 shows the threshold voltages (V_{th}) of the $Al_2O_3/Ta_2O_5/Al_2O_3$ and $Al_2O_3/TaAlO_4/Al_2O_3$ films as a function of the number of program/erase cycles in an endurance test. Generally, the retention property can explain two aspects of the stored charge, the preservation time and memory window degradation during program/erase (P/E) operation. However, the preservation time of a stored charge is less problematic than the memory window degradation issue. Since the loss of a stored charge is time-dependent and the rate of decrease is small, researchers or manufacturers

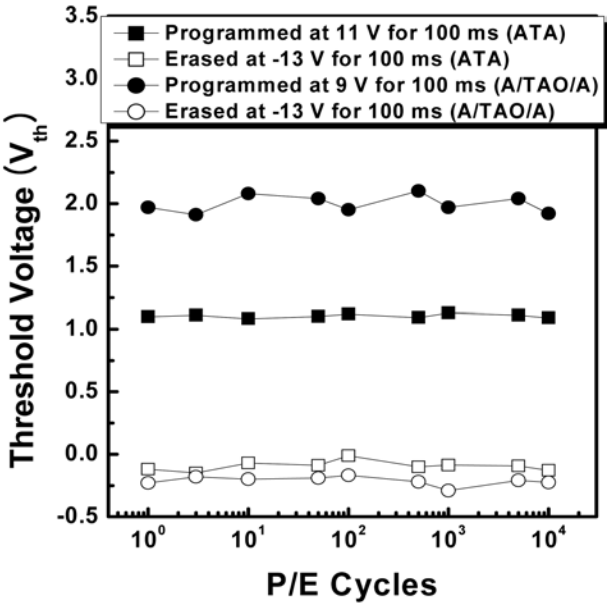

Fig. 5. Threshold voltage (V_{th}) changes of the Pt/Al_2O_3/Ta_2O_5/Al_2O_3/Si and Pt/Al_2O_3/$TaAlO_4$/Al_2O_3/Si capacitors after program/erase cycle tests.

can sufficiently forecast a device's lifespan.

The number of P/E cycles is a major issue in the ITRS roadmap. According to a previous study [25], a 40% decrease of the initial memory window over 10 years was equivalent to 10^{6-7} P/E cycles, meaning that this decrease occurred after the performance of 10^{6-7} iterations of the program/erase operation. In this study, 10^{6-7} P/E cycles was considered to be equivalent to 10 years of device use. In other words, a device can be used for at least 10 years if it passes the 10^{6-7} program/erase cycle test. Of course, the memory window value after the P/E cycle test will likely decrease to up to 40% of the initial value, however the device can still be used if the final memory window value is relatively wide.

We performed a retention study by taking repeated measurements of program and erase operations; Figure 5 shows the results. Memory windows did not change after up to approximately 10^4 P/E cycles. The memory window values of the Al_2O_3/Ta_2O_5/Al_2O_3 (1.225 ΔV_{th}) and Al_2O_3/$TaAlO_4$/Al_2O_3 (2.197 ΔV_{th}) films decreased by 0.49 and 0.88 ΔV_{th}, respectively. Based on our tests, the memory characteristics of films with Ta_2O_5 as the trap layer are not suitable for replacement of the ONO (SiO_2-nitride-SiO_2) structure, but the memory characteristics of films using $Ta_1Al_1O_4$ as the trap layer may be acceptable due to recently improved sense amplifiers. Overall, the results of this study indicate that A/TAO/A films possess better properties than ATA films and are feasible for use in flash memory devices as a replacement for ONO structures.

Conclusions

SONOS is the most widely studied structure for use as a CTD (Charge Trap Device). However, in the context of the scaled down size of modern devices, SONOS devices have problems such as high erase power and poor retention properties. In this paper, we studied the memory characteristics of multilayer films with Ta_2O_5 and $TaAlO_4$ as the trap layer in order to address these problems and to identify replacements for the conventional ONO structure. The memory windows of the ATA and A/TAO/A films were 1.225 and 2.197 ΔV_{th}, respectively, and the optimized electrical conditions of the A/TAO/A films were found to be superior to those of the ATA films. Interfacial layers ($AlSiO_3$) were observed in both the ATA and A/TAO/A films, and their thicknesses were determined to be 12.5 Å (ATA) and 21.8 Å (A/TAO/A), respectively. Initial memory windows were sustained after 10^4 program/erase cycles, which suggests that both films can be used in next generation, non-volatile memory devices without causing reliability problems. However, based on superior electrical properties (i.e., memory window, program/erase conditions and program/erase maintenance), the A/TAO/A films are more suitable as replacements for conventional ONO structures than ATA films.

Both proposed device structures have two strong advantages over the conventional ONO (SiO_2/Si_3N_4/SiO_2) structure. First, the results of the P/E cycle test [memory window; V_{th}(program)-V_{th}(erase)] for both of the proposed films were superior to those for the conventional ONO structure. Generally, the conventional ONO has a memory window of about 1 eV. However, our ATA and A/TAO/A structures had memory windows of about 1.22 eV and 2.19 eV, respectively. In particular, the memory window of the A/TAO/A structure was far superior to that of the ONO structure.

Second, the ONO structure has many limitations. According to Moore's law or the ITRS road map, semiconductor devices should be scaled-down for better performance. However, tunnel oxide thickness in the conventional ONO structure cannot be reduced to less than 3 nm due to problems of charge leakage, low retention, etc. Therefore, a material other than SiO_2 must be used for the tunnel oxide in scaled down semiconductor devices. One solution to this problem is the use of high dielectric constant materials that have a dielectric constant higher than SiO_2. The use of high-k materials that have the same EOT (equivalent oxide thickness) as SiO_2 but a greater physical thickness solves the SiO_2 thickness problem, thereby allowing the continuous scale-down of semiconductor devices to proceed.

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